DVP

NEW TECHNICAL THEORY
FOR SERVICING

DVP-M35/S300/S305/S315/ S500D/S505D/S715

OPERATION MANUAL

CD/DVD PLAYER

SONY

Contents

1. Outline

This guidebook describes the DVD-Video.
It also describes the functions not used in the DVP Series.
For the functions used in the DVP Series, refer to Secions 2 to 5, or Service Manual.

1-1. Series line-up

① Basic Dolby digital model
DVP-S500D NTSC U/C specifications (120V)
DVP-S500D NTSC General overseas specifications (110 to 240V)
DVP-S501D NTSC Japan specifications (100V)
DVP-S505D PAL/NTSC Hong Kong specifications (230V)

*AC3 : 5.1ch OUT (With built-in decoder)
*Output terminal : S terminal, video, audio x2
Color difference output x1

② 280 size model
DVP-M30 NTSC Japan specifications (100V)
DVP-M35 PAL/NTSC China specifications (230V)
DVP-M35 PAL/NTSC Hong Kong specifications (230V)
DVP-M35 PAL/NTSC General overseas specifications (110 to 240V)
DVP-M35 PAL/NTSC Singapore specifications (230V)

*Pixy size
*Output terminal: S terminal, video, audio x2

③ Basic model
DVP-S300 NTSC U/C specifications (120V)
DVP-S300 NTSC General overseas specifications (110 to 240V)
DVP-S305 PAL/NTSC China specifications (230V)
DVP-S305 PAL/NTSC Taiwan specifications (110V)
DVP-S305 PAL/NTSC General overseas specifications (110 to 240V)
DVP-S305 PAL/NTSC Singapore specifications (230V)
DVP-S315 PAL/NTSC European specifications (230V)
DVP-S315 PAL/NTSC Great Britain specifications (230V)
DVP-S715 PAL/NTSC European specifications (230V)
DVP-S715 PAL/NTSC Great Britain specifications (230V)
DVP-S715 PAL/NTSC Australia specifications (230V)

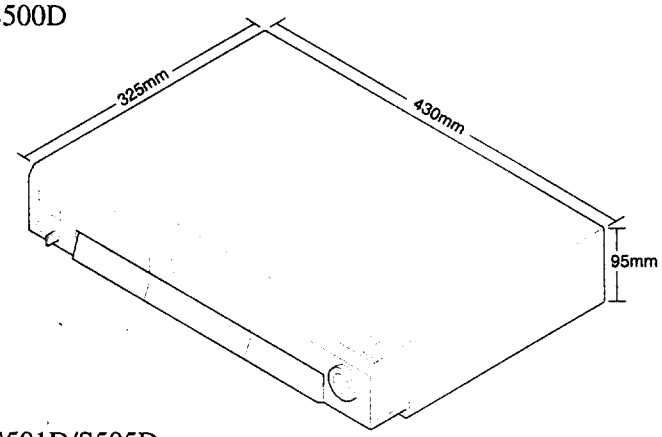
*Output terminal AC3
21P Euro (DVP-S315, S715)
S terminal, video, audio x1

Note: Video-CDs recorded in the PAL format can be played only by general overseas specifications models.

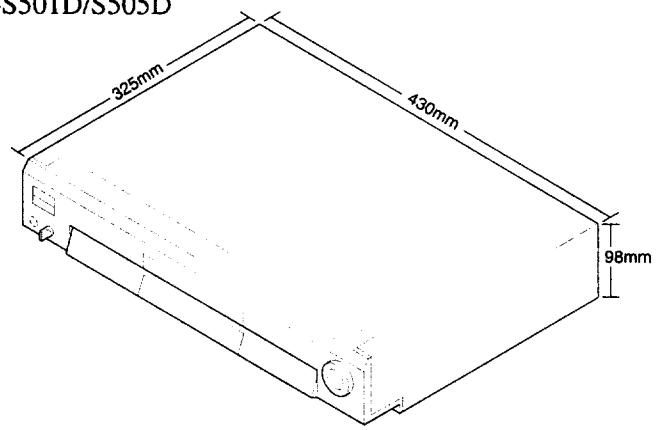
1-2. External appearance diagram

① Basic Dolby digital models

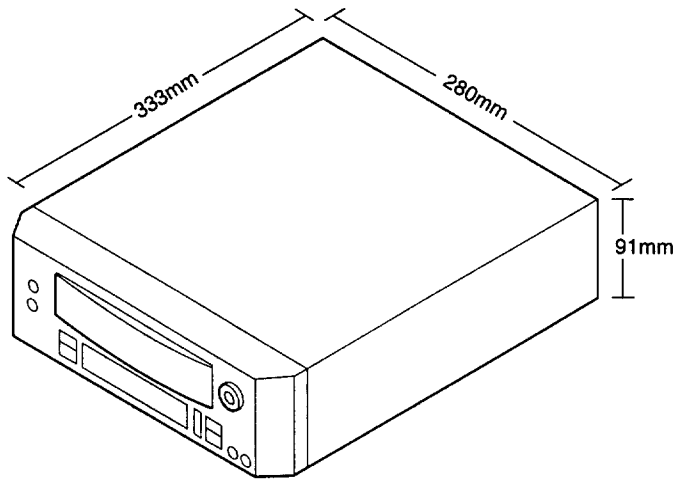
DVP-S500D



DVP-S501D/S505D

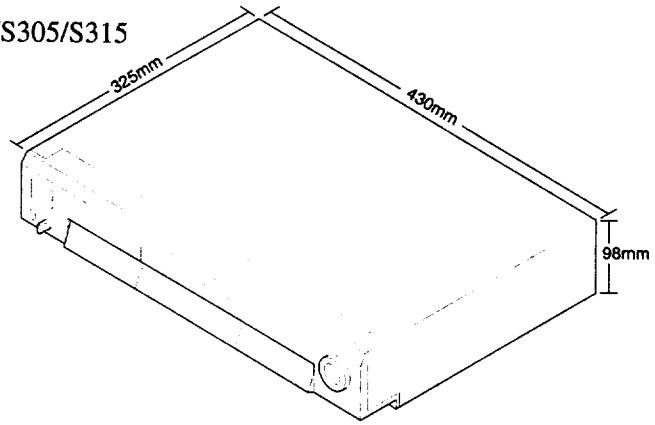


② 280 size models

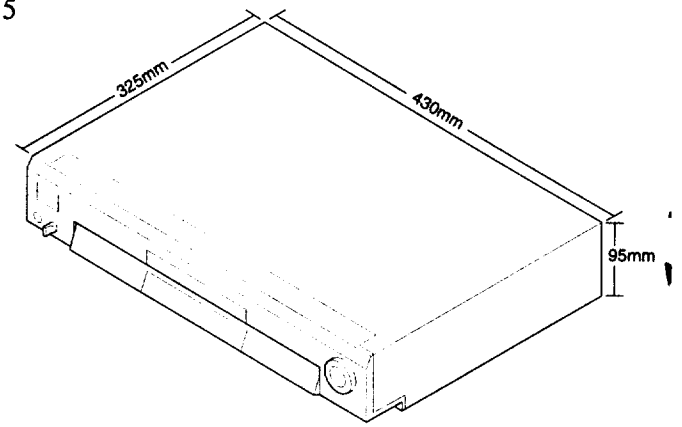


③ Basic models

DVP-S300/S305/S315

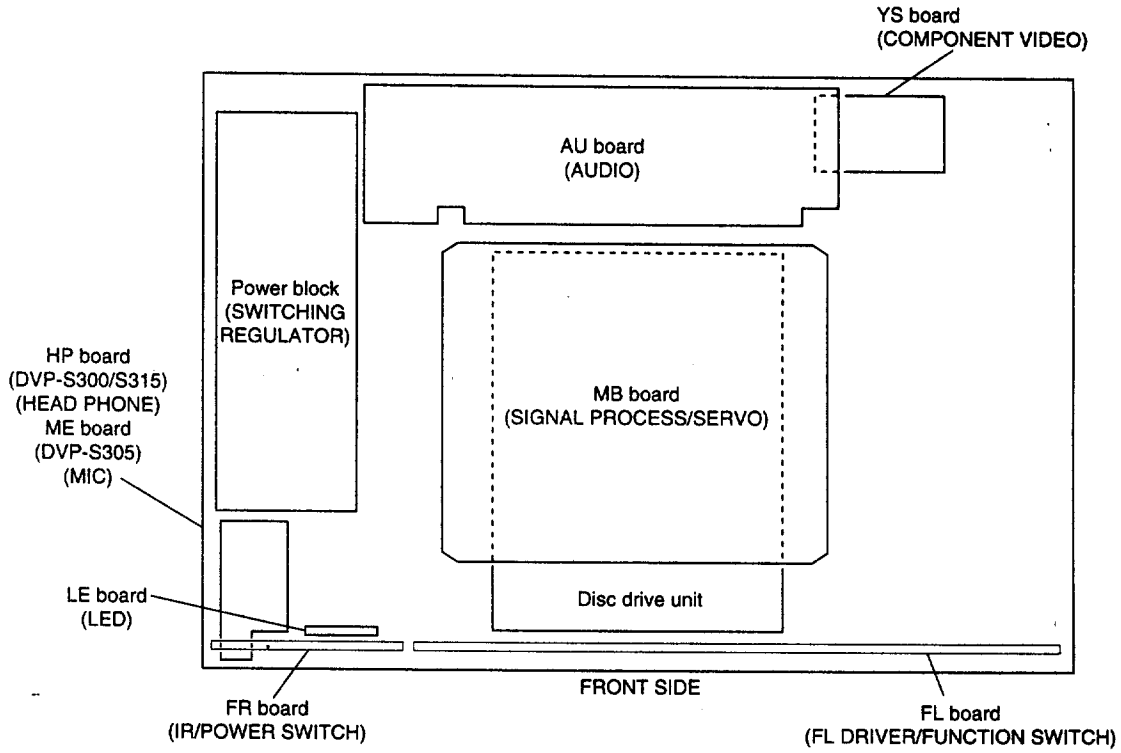


DVP-S715

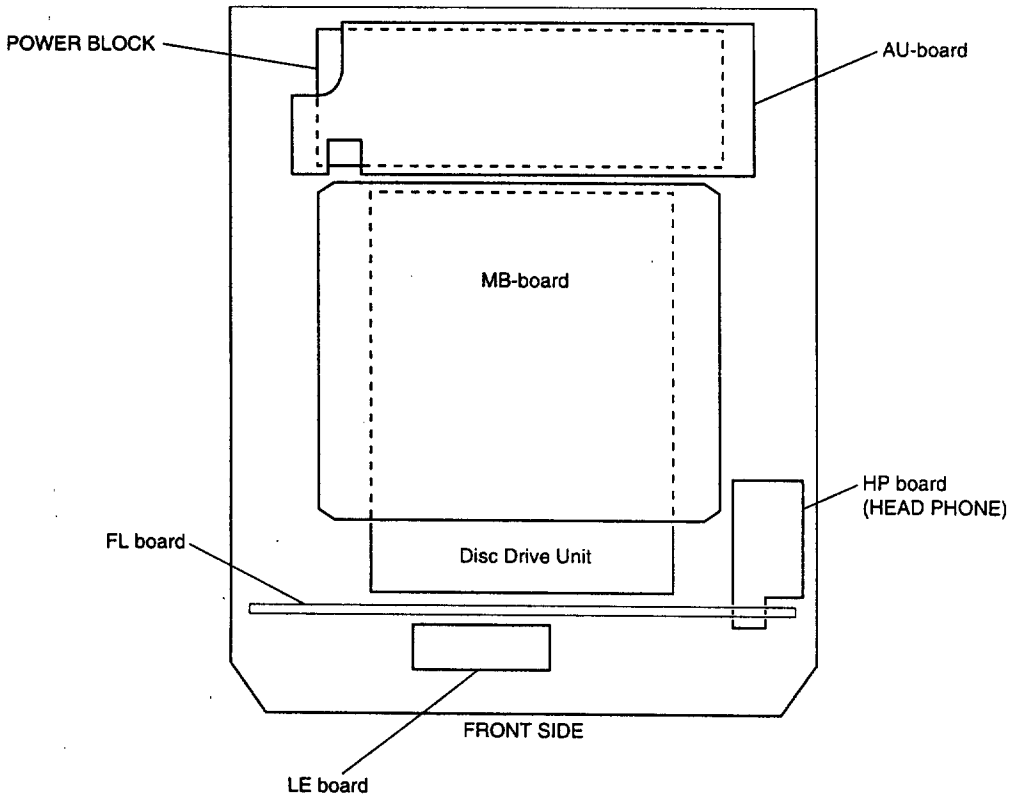


1-3. Internal appearance diagram (top view)

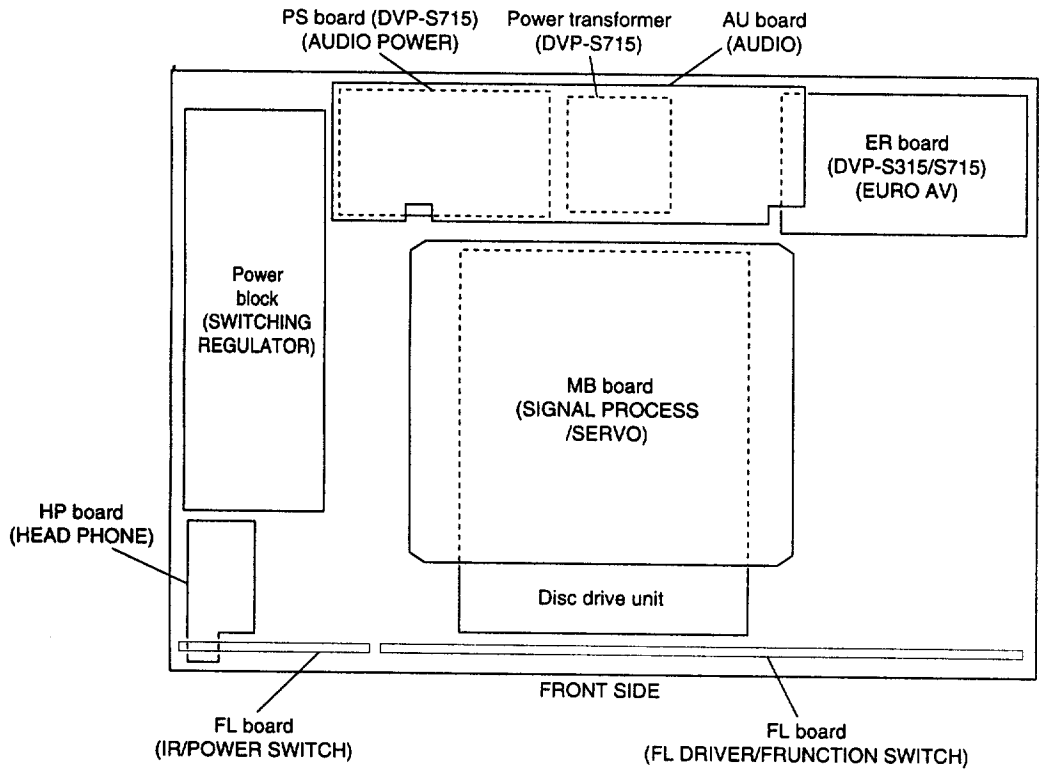
① Basic Dolby digital models



② 280 size models



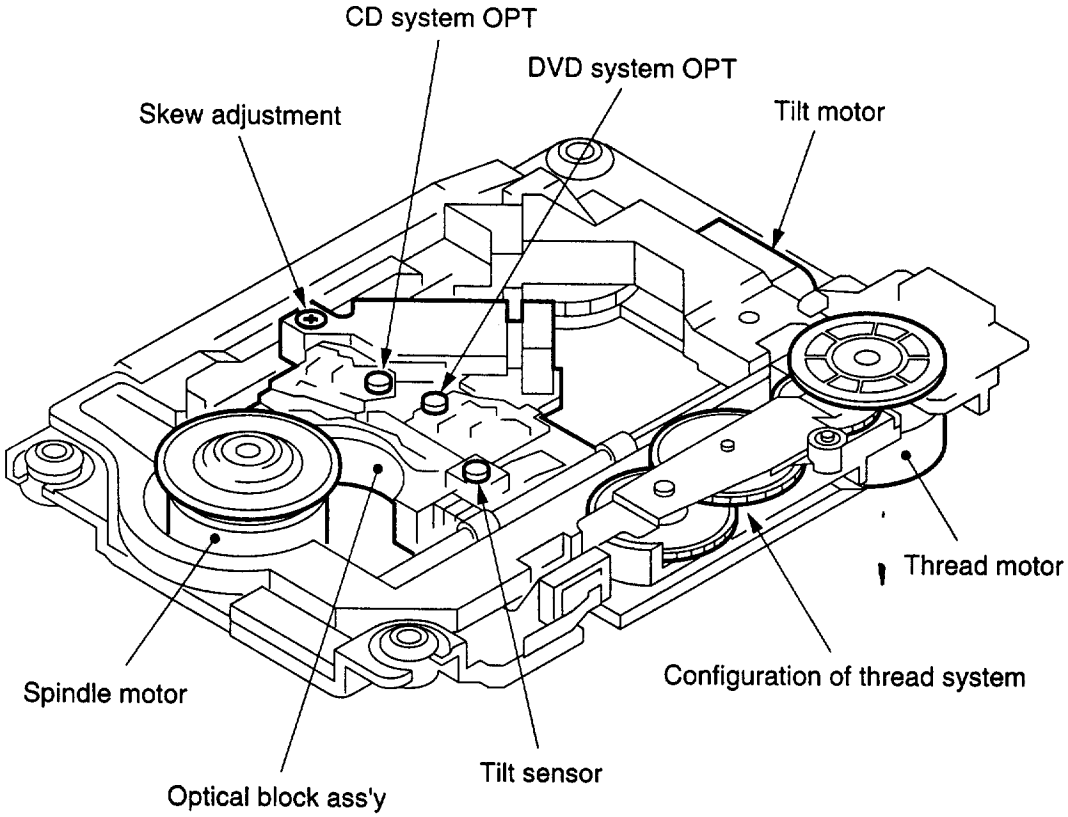
③ Basic models



1-4. Disc drive unit

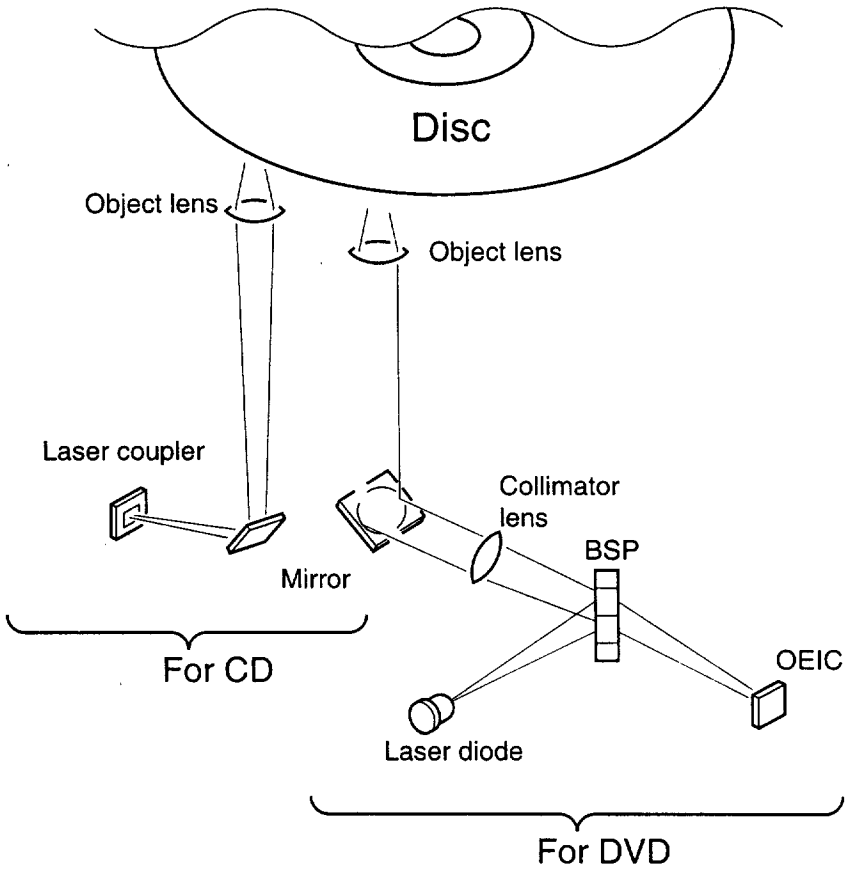
1) Configuration of disc drive unit.

[Optical block specifications]

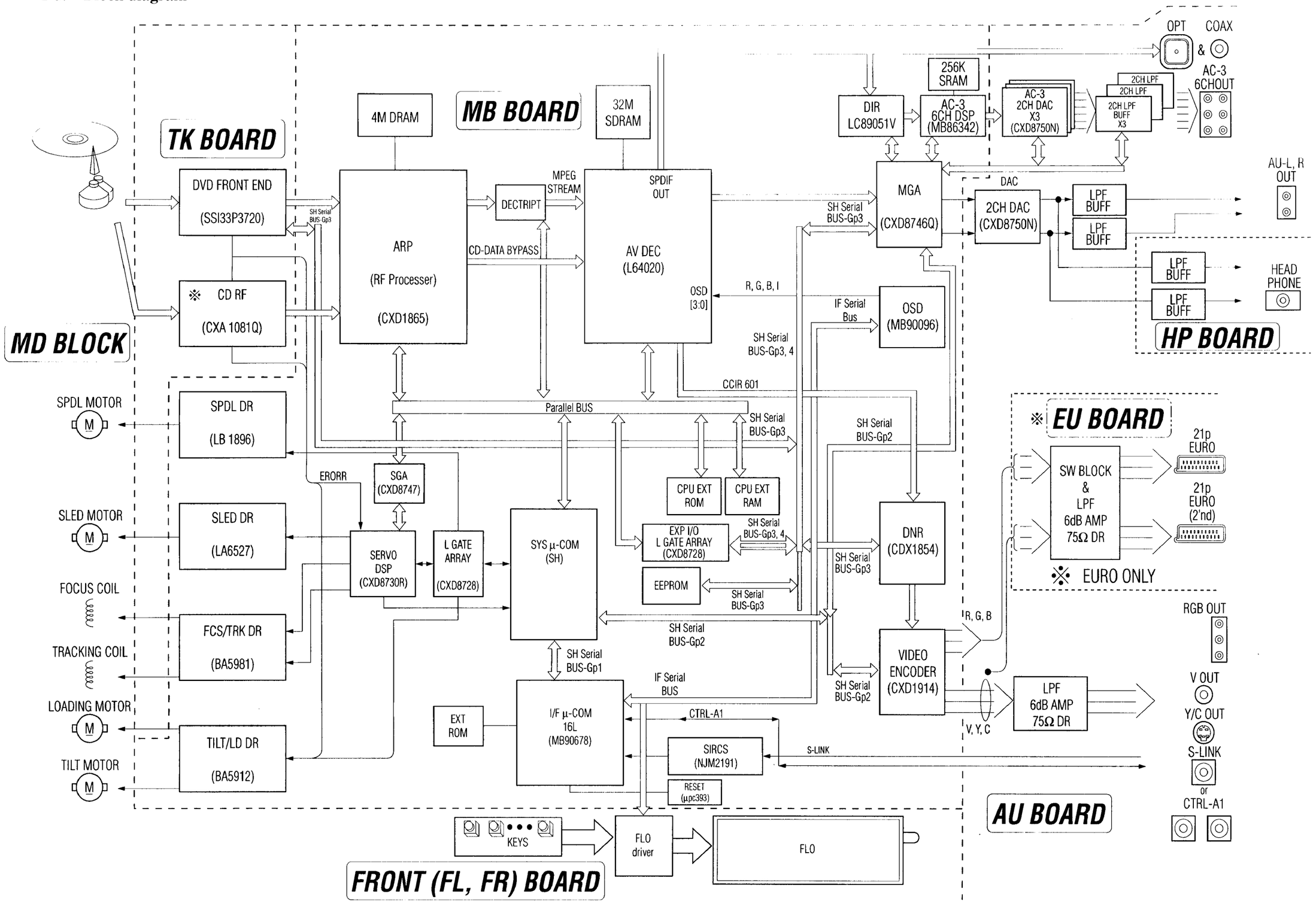


Specification	DVD system OPT	DC system OPT
Optical system	Non-deflection, unlimited optical system	Non-deflection, limited optical system (laser coupler)
Drive unit	2-shaft	2-shaft
Object lens	Glass	Plastic
Focus error	Stigmatic system	Differential 3-division system
Tracking error	DPD system	TPP system
Laser beam	650nm	780nm

2) Optical route diagram



1-5. Block diagram



2. Signal Processing Block

Block which performs various signal processings from the RF front end to the output of the audio signal and video signal.

2-1. DVD RF Front End

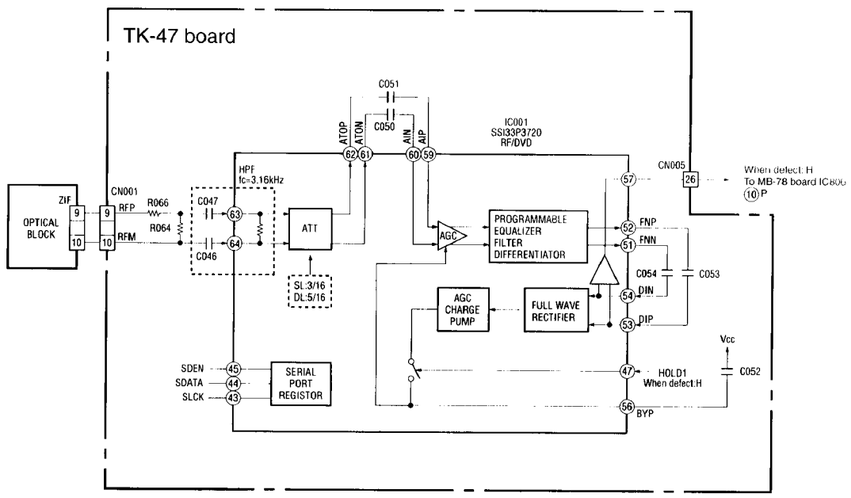


Figure 2-1. TK-47 Board IC006 SSI33P3720 RF/DVD

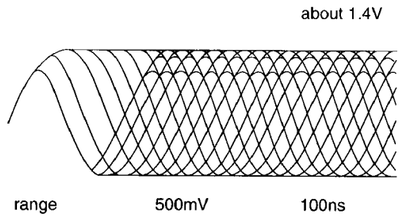


Figure 2-2.
RF (eye pattern) waveform at DVD disc
TK-47 board CN005㉖P

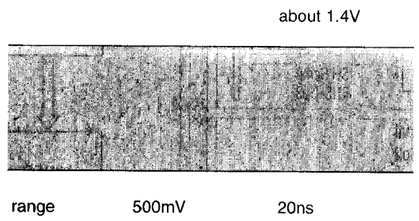


Figure 2-3.
RF envelope waveform at DVD disc
TK-47 board CN005㉖P

2-1-1. Attenuation of OP Output Signals

The RF signals (RFP, RFM) output from OP for DVD are attenuated by R066 and R064 so that they satisfy the input amplitude allowable level of IC006 in the post stage.
(About $1V_{PPD}$ (*3) for SL (*1) disc. In actual, only the RFP signal is output because RFM signal is connected to the ground in the OP block.

2-1-2. HPF

Low frequency component of the attenuated RF signal is removed by a high pass filter (HPF) that cuts off the frequency (about 3.16kHz) determined by the input impedance of C046, C047, and IC006, then it is entered to the IC001.

2-1-3. RF Front End Processing: IC001 SSI33P3720

(1) ATT block

The RF signal entered from IC006 RFP㊸ and RFN㊹ is entered to the ATT block. In this block, this processing is executed to attenuate the signal below signal amplitude level determined according to the specification (about $200mV_{PPD}$, determined depending on AGC input allowable level) in order to utilize high performance of IC.
After processing, the signal is output from IC006 ATOP㊷ and ATON㊶.

ATT: Set to 3/16 for SL disc, or 5/16 for DL (*2) disc.

These are operated by the command register set via serial interface.

(2) AGC block

ATT output IC006 ATOP㊷ and ATON㊶ are processed below AGC allowable level as mentioned above, then they are AC-coupled by C050 and C051, and entered respectively to AGC block input IC001 AIP㊾ and AIN㊿.
The AGC block controls gain of AGC amplifier so that constant input signal ($1V_{PPD}$) is supplied to the IC006 DIP㊸ and DIN㊹. The AGC compares full-wave rectified input signal to IC006 DIP㊸ and DIN㊹ with reference level, and repeats decay and attack while keeping a balance with the product of current by time so as to attain the optimum gain.

Decay: When input signal to IC006 DIP㊸ and DIN㊹ is below $1V_{PPD}$, C052 (C_{BYP}) is discharged with 4μA decay current. In this case, AGC amplifier gain gradually increases.

Attack: When input signal to IC006 DIP㊸ and DIN㊹ is over $1V_{PPD}$, C052 (C_{BYP}) is charged with 0.18mA attack current. In this case, AGC amplifier gain gradually decreases.

The input signal to IC006 DIP㊸ and DIN㊹ is a signal processed after EQ block mentioned later.

*1: Single Layer disc *2: Dual Layer disc *3: Peak to Peak Differential

(3) EQ block

The EQ block is a programmable equalizer filter differentiator block.

The DVD format is premised on the EQ and requires high frequency signals to be boosted. This block equalizes RF signal to get optimum RF signal by combining LPF and EQ (boost), as shown in Figure 2-4. LPF is defined as -3dB band width without boost. If the amount of boost is set to a certain value, the gain at cut-off frequency is as follows:

Gain (at cut-off frequency) = -3dB + Boost amount [dB]

Also, LPF is used as a prefilter for the A/D converter provided in the input stage of RF block of IC in the post stage (MB78 board IC770).

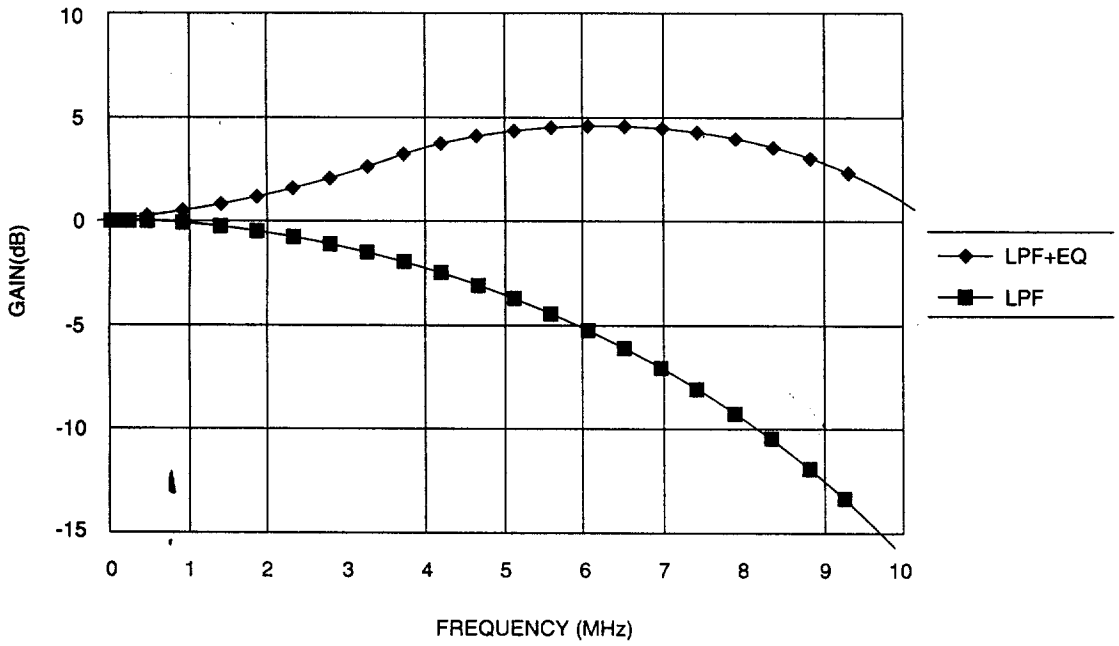


Figure 2-4. Frequency characteristics (EQ+LPF)

These cut-off frequency and boost amount of LPF are operated by the command register set via serial interface.

The RF signal processed in this block is output from IC006 FNP㊷ and FNN㊶. This signal is entered to IC006 DIP㊸ and DIN㊹ and rectified in full wave, then compared in the AGC block. The RF signal output from IC006 SIG㊼ is then transmitted to the RF signal processing block IC806 in the post stage.

(4) Serial interface

Various values of IC006 are set to internal serial port register via serial interface. Actually, they are set by three signals from the L G/A IC804. Signals are SDEN㊺, SDATA㊹, and SCLK㊸, and its timing chart is shown in Figure 2-5.

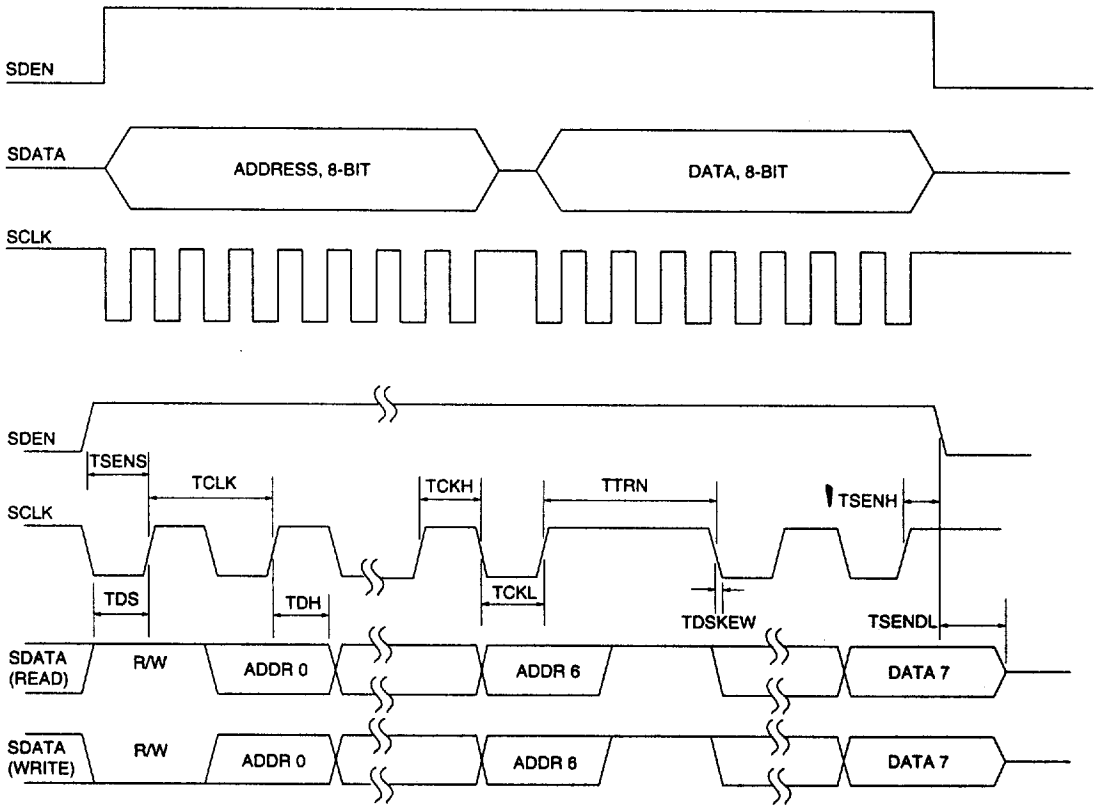


Figure 2-5. Timing chart

2-2. CD RF Front End

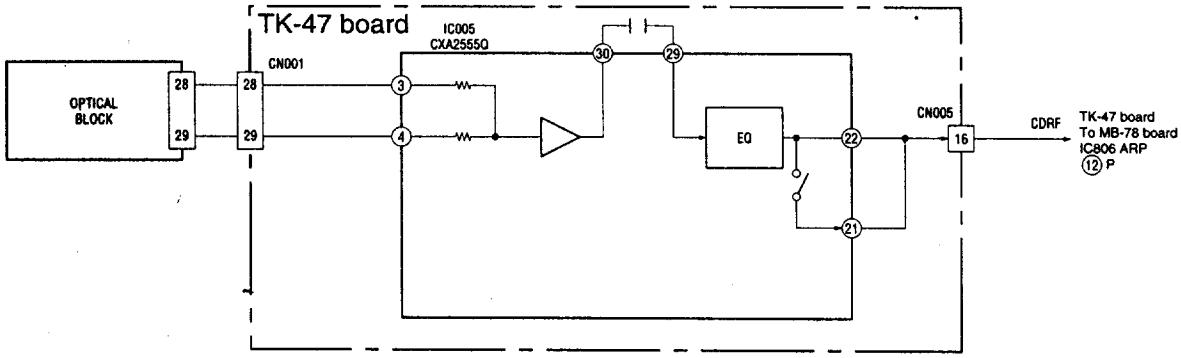


Figure 2-6. TK-47 board RF/CD

The RF signal output from the CD OP is input to IC005 ③ and ④, and transmitted to IC806ARP of the MB-78 board via the amplifier, equalizer.

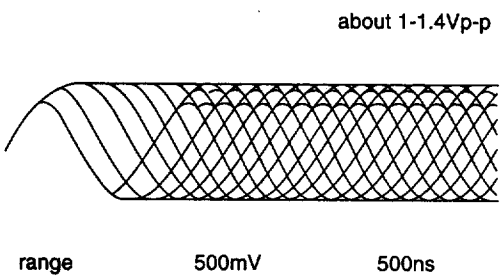


Figure 2-7.
RF (eye pattern) waveform at CD disc
TK-47 board CN005⑯P

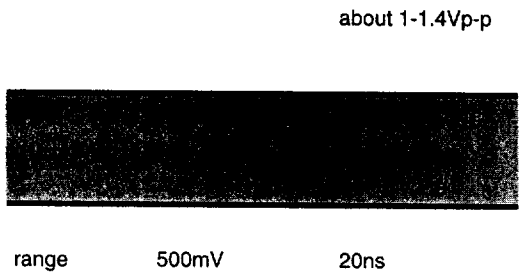


Figure 2-8.
RF envelope waveform at CD disc
TK-47 board CN005⑯P

2-3. RF Signal Processing Block

The block is composed of the IC806 ARP (CXD1865R) and IC810 4Mbit DRAM (μPD424260) of the MB-78 board.

In the case of the DVD, the ARP is input with the AGC and RF equalize-processed DVD-RF signal at the IC006 analog front end (SSI33P3720) of the TK-47 board. In the case of the CD-DA and video-CD, it is input with the CD-RF signal from IC005 of the TK-47 board.

In the ARP, first RF signal processing such as asymmetry correction, adaptive equalization, and sync clock extraction by the RF-PLL are carried out so that the signal becomes binary data synchronized with the PLL clock. This data is EFMPlus demodulated (DVD)/EFM demodulated (CD-DA and video-CD) in the demodulator, subjected to frame/sector sync detection, address detection, and protection, and sent to the buffer memory controller.

In the case of the DVD and video-CD, the ARP is linked to the ECC core, built-in and external memories, and output controller to carry out error correction, descrambling, EDC detection, navigation information detection (DVD only), and output data flow control, etc. The data output in this way is then sent to the decrypt block in the next stage.

This is the same for the CDDA. The ARP is linked to the built-in and external memories, and CDDA signal processing block to carry out error correction, output data flow control, etc. The signal is then muted and corrected by the CDDA signal processing block, and then sent to the IC203AV decoder (L64020).

For all of these disks, RF jitter is calculated by the RF signal processing block, and this information is used for adaptive control of the servo DSP via the CPU.

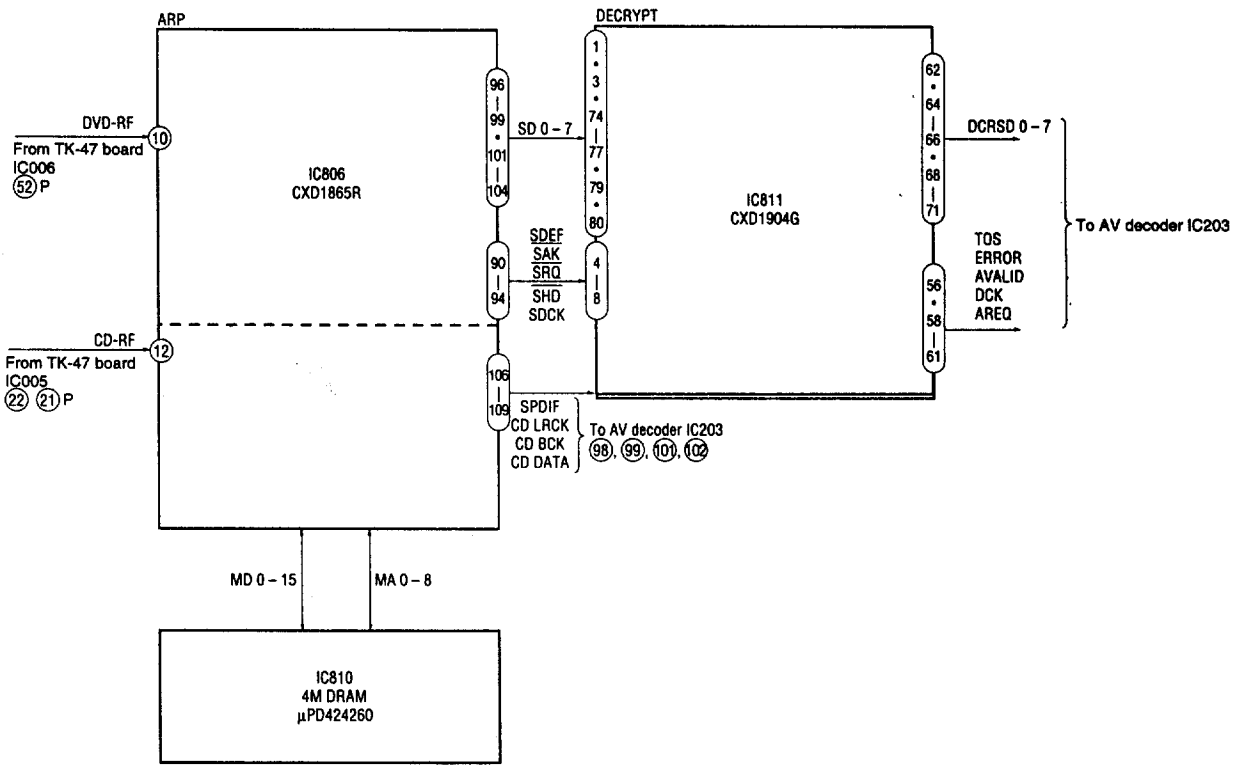


Figure 2-9. MB-78 board RF processor, decrypt

2-4. Decrypt Block

Data sent from ARP is subject to decoding of the digital copy protection for preventing illegal copy determined by DVD standards at IC811 (CXD1904), and then sent to the AV decoder in the post stage.

2-5. AV Decoder Block

Composed of two 16M SDRAMs (IC201, 202MB81117622) and AVDEC (IC203, L64020), it is used to decode DVD/VCD data (MPEG stream) from the decrypt.

After decoding, the video signal is letter box converted, and output together with the subpicture and OSD signals.

The audio signal is decoded for the two channels AC3/MPEG/LPCM and output. Separately AC3/MPEG compressed data is output as IEC958.
The CD data from ARP is bypassed inside and output from the audio output.

2-6. OSD Block

IC207 of the MB-78 board (MB90096) outputs the player menu, and adds it to the video signal inside the AV decoder IC203 (L64020).

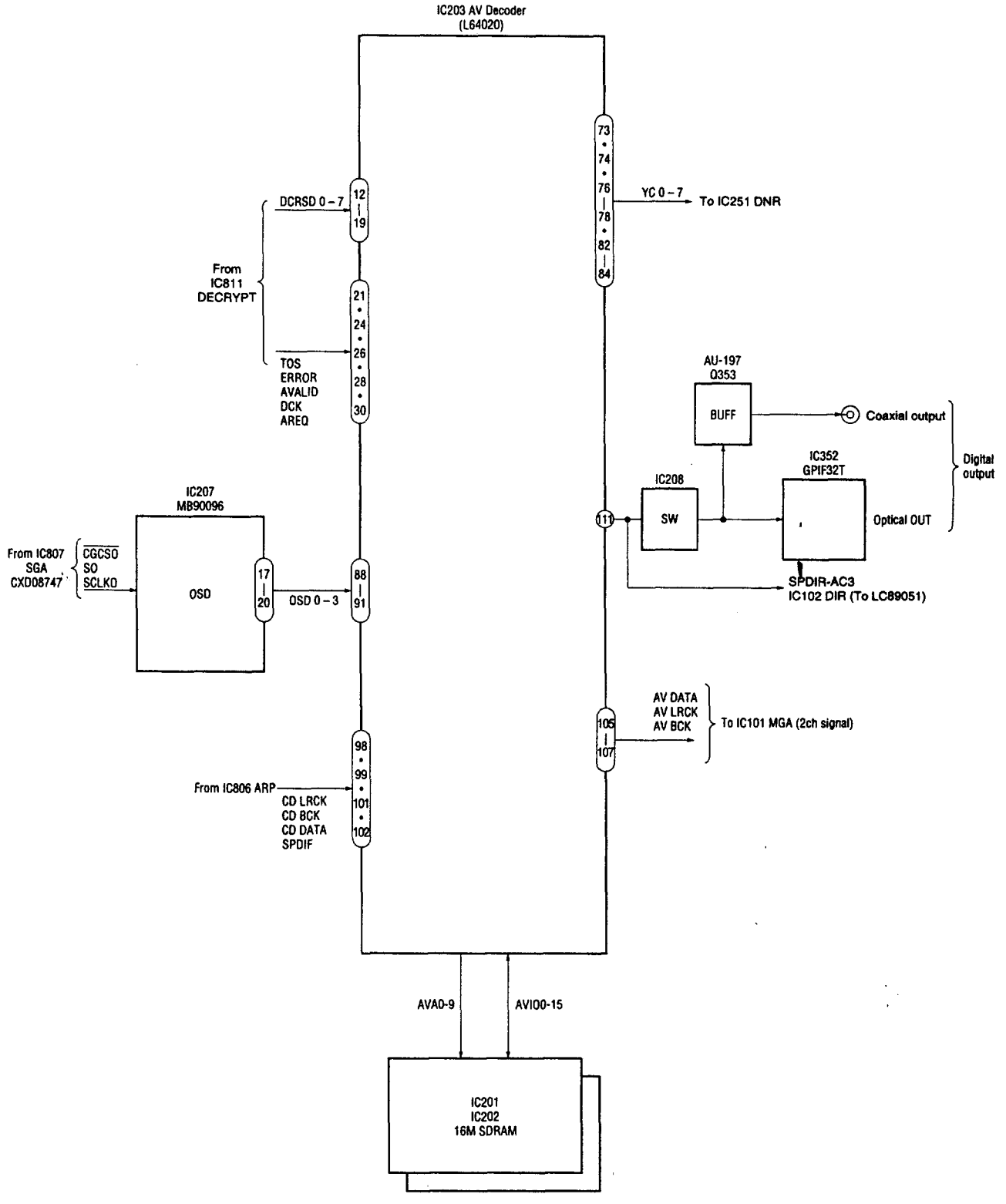


Figure 2-10. AV Decoder, OSD

2-7. DNR, Video Encoder Blocks

The video data from the AV decoder is sent to IC251, DNR (CXD1854), subjected to video noise reduction, and sent to the IC252 video encoder CXD1914 in the post stage. The video data is converted to NTSC/PAL video signal (color difference signal/S-Y, S-C/composite) here.

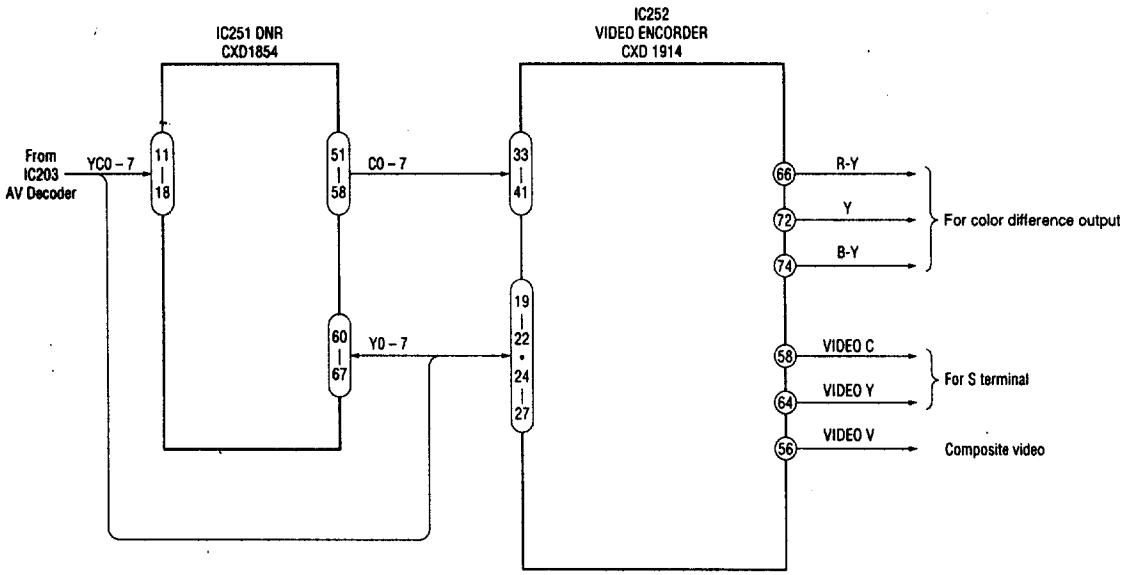


Figure 2-11. DNR video encoder

Signals are output externally after passing through the 75 Ω driver.

2-8. Clock Generator Block

The IC209 CXD8696PLL IC generates 27 MHz, and using this as the master clock, generates the system clock for audio decoding.

System Clock	384fs	768fs
CD/VCD	16.9344 MHz	33.8688 MHz
DVD	18.4320 MHz	36.8640 MHz

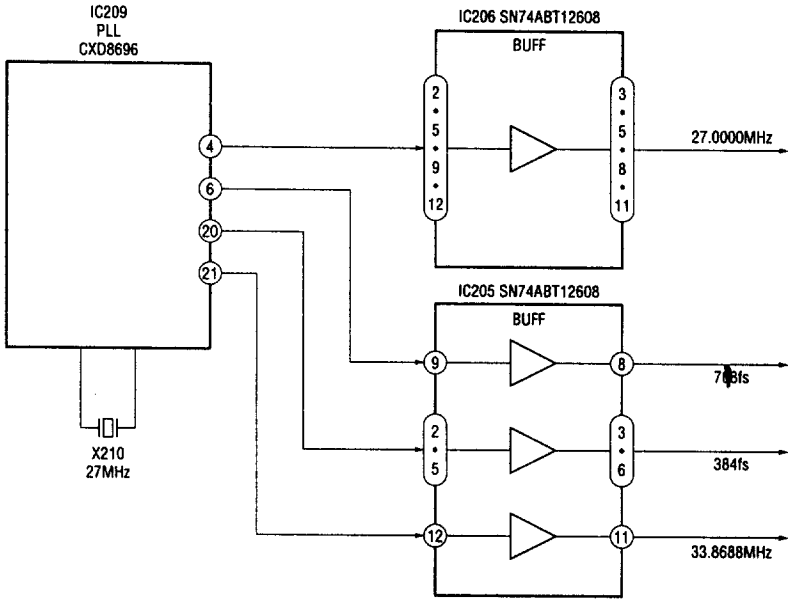


Figure 2-12. Clock generator

2-9. AC-3 Decoder Block

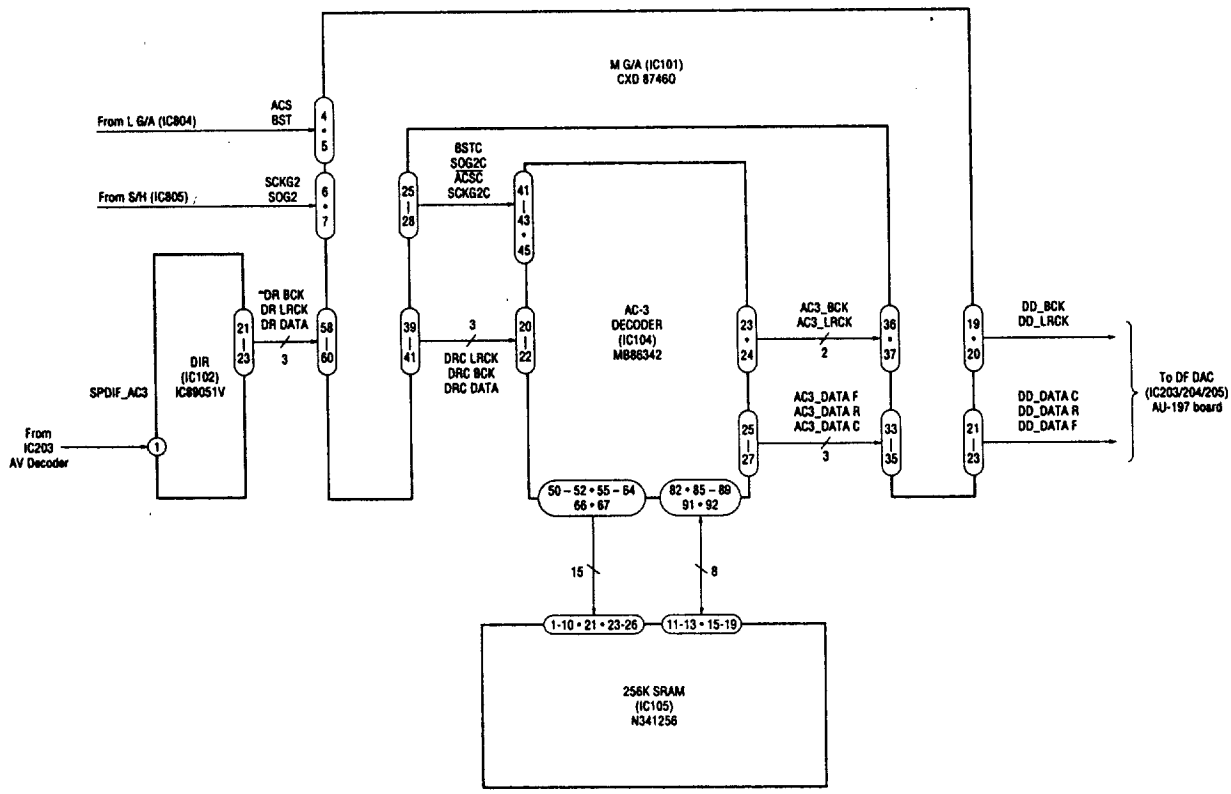


Figure 2-13. AC-3 Decoder

The SPDIF_AC3 (Dolby Digital Bit-Stream) audio data output from AVDEC is input to the AC-3 decoder (IC104) via DIR (IC102) and M G/A (IC101). In the AC-3 decoder (IC104), the data is processed for three lines, and sent to the AU-197 board DF/GAC via the M G/A (IC101).

2-10. Audio L and R 2ch Signal Block

The audio signal data for 2 channels of the MB-78 board AV decoder IC203 (L64020) is passed through IC101MGA, passed through the digital filter in the AU197 board IC215 (CXD8750), converted to analog signal in the DAC, and passed through the LDF to become the line out signal.

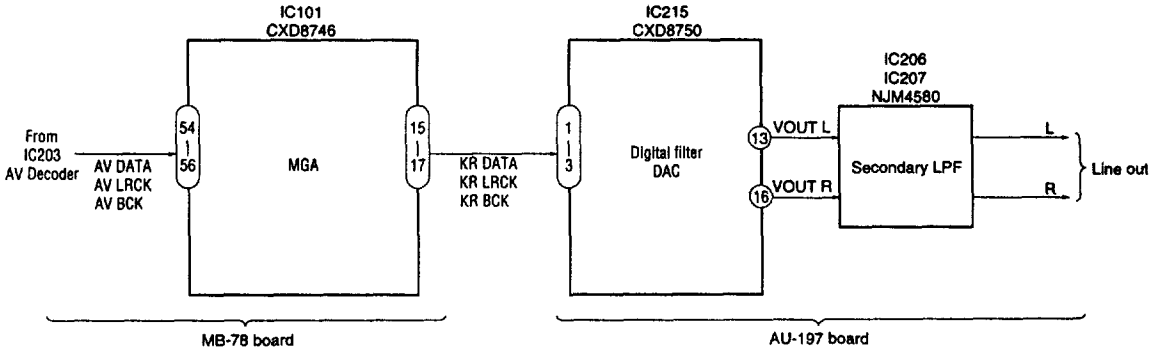


Figure 2-14. 2ch signal block

The line out signal line is also branched out to IC214 to become the headphones amplifier output.

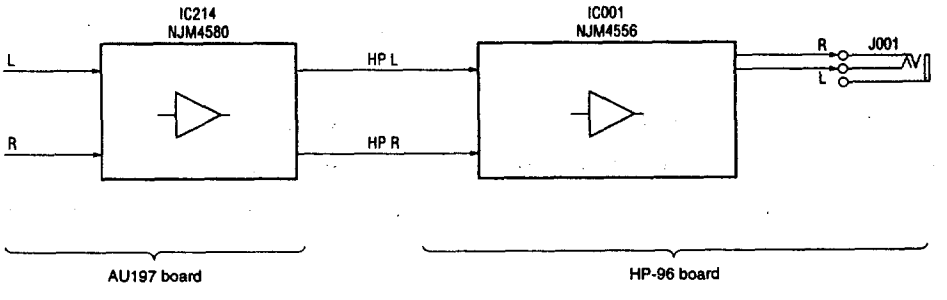


Figure 2-15. Headphones amplifier

2-11. Audio 5.1ch Signal Block

The AC3 decoded signal DD-DATA C/R/F output from the MB-78 board IC101 MGA (CXD8746) is input together with DD BCK and DD LRCK to IC203, IC204, and IC205 (CXD8750) of the AU-197 board, passed through the digital filter, and converted to the analog signal in DAC.

The front L and R signals are then passed through IC203 of the AU-197 board, gain-controlled at IC353 (BU4053B), and noise-eliminated at the secondary LPF IC208, IC211 (NJM4580) to become the external output of the front L and R.

The sound L and R, and center sub woofer signals are passed through IC204 and IC205 without being gain-controlled, and noise-eliminated in the secondary LPF IC209, IC212, IC210 and IC213 (NJM4580) to become the external output.

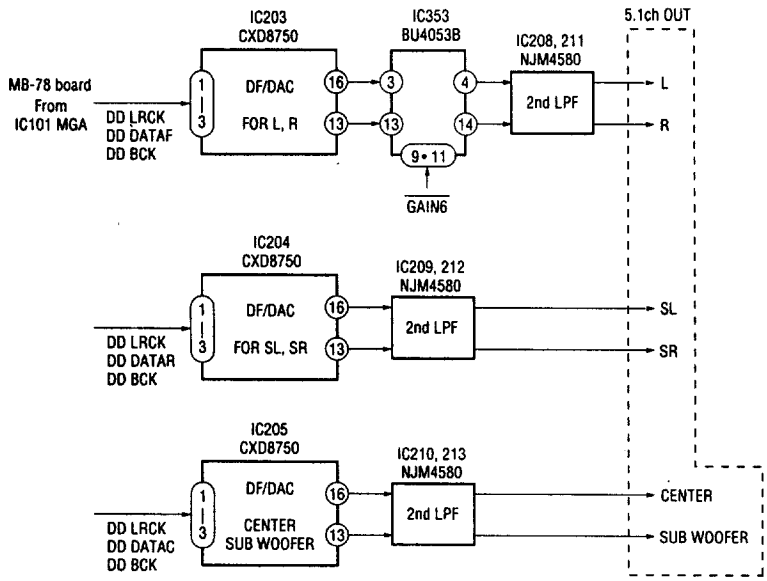


Figure 2-16. 5.1ch Signal Block

2-12. DVP-S715 AU-205 Board Block Diagram

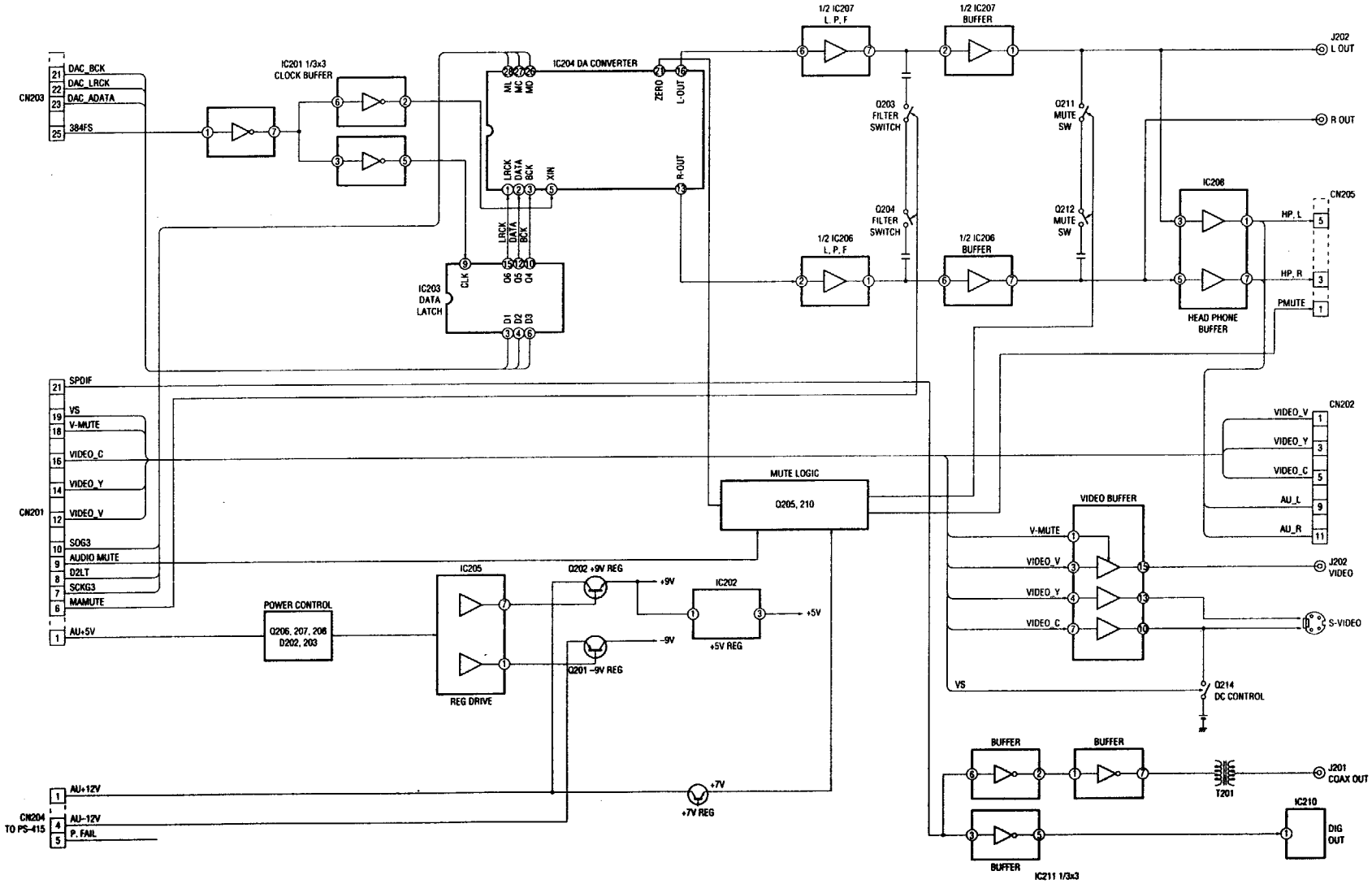


Figure 2-17

2-13. System Control Block

The system controller is composed mainly of the IC805 (HD6437034) SH microcomputer, and IC807 (CXD8728) large gate array, IC802 (HM62812) 1M SRAM, ICS803 8M FLASH memory, and IC807 (CXD8747) small gate array, etc. It serves to control the overall servo system.

2-14. Interface Control Block

The interface controller is composed of the IC604 (MB90T678) I/F microcomputer, IC608 (μPD432568) 256K SRAM, IC601 (SN74HC373), and ICS603 external ROM. It sends various commands to the SH microcomputer based on the switch information from the FL board and FR board, receives the current information from the SH microcomputer, and displays on the FL tube display.

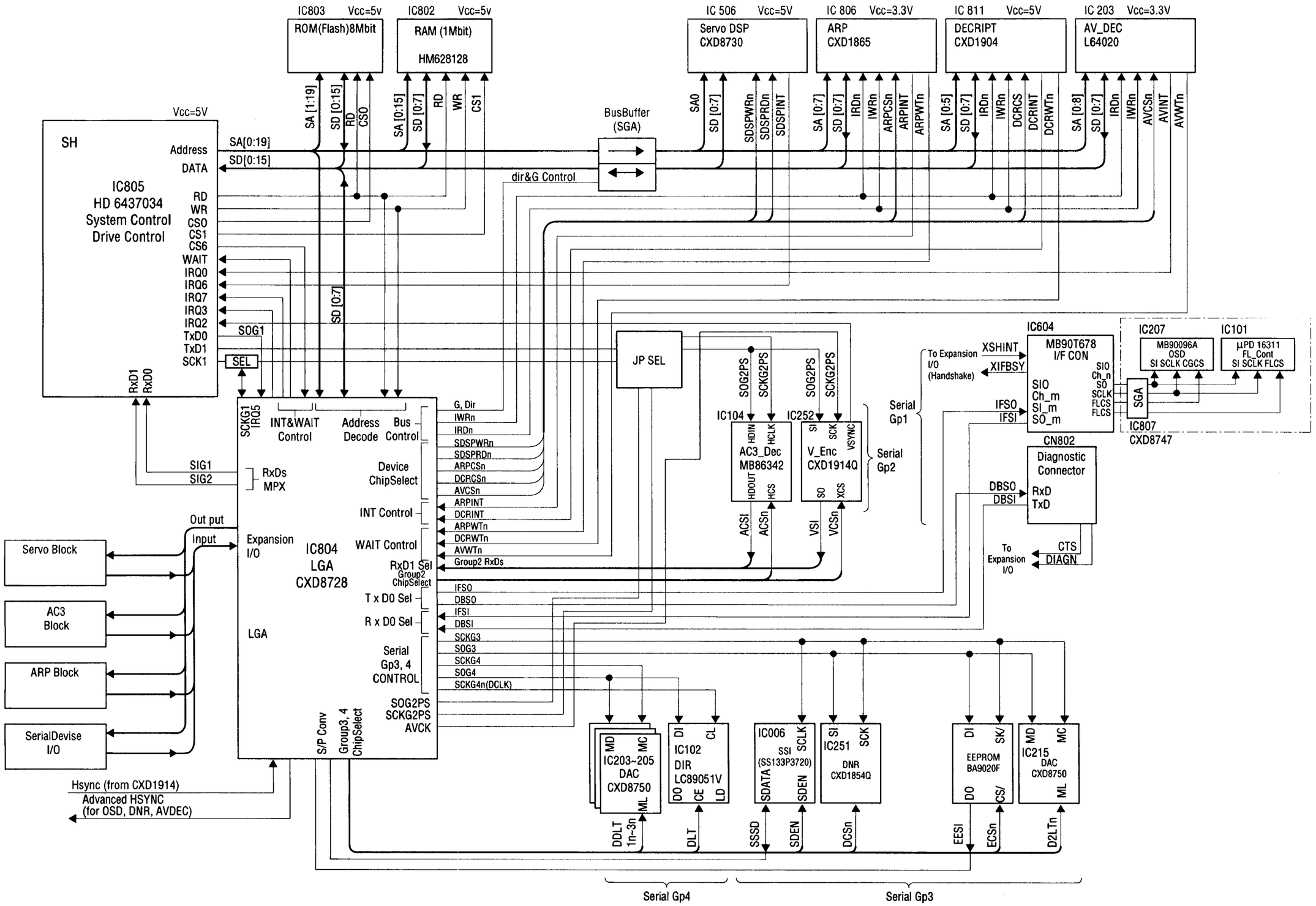


Fig. 2-18. System Controller Peripheral Device Control Block Diagram

3. SERVO BLOCK

3-1. General Description of Servo Circuits

3-1-1. Optical Pickup Control

Dedicated optical pickups for DVD and for CD and video CD are provided. The focus and tracking servo gains are automatically adjusted for every disc loading so that the gains are constant for every disc to be played.

3-1-2. Sled Control

Two pickups for DVD and CD/video CD are placed on the same sled, and the position is controlled with one sled motor. The sled motor is attached with a speed detector utilizing the Hall element, and a sled speed fluctuation due to mechanical load variations is minimized by applying the speed servo control (feedback control).
The sled motor used is a DC motor with a brush.
The servo system circuit is used for both DVD and CD.

3-1-3. Spindle Control

One 3-phase brushless motor controls all disc rotations. The rotation detection pulses (FG: Frequency Generator) utilizing the Hall element are used for control.

3-1-4. Tilt Control

The optical pickup is controlled so that the optical axis is perpendicular to the disc; when DVD is played, it is controlled so that the time axis variation (jitter) of RF signal becomes minimum.
At the start of DVD play (before RF signal is output), optical sensor detects the tilt angle of disc and the optical pickup is controlled so that the optical axis is perpendicular to the disc.
The servo system circuit is used for both DVD and CD. At DVD, it always performs tilt operation, but at CD, it operates only during start-up and stops at the tilt position during playback.

3-1-5. Disc Loading and Chucking

One DC motor drives the tray in-out motions, and chucking of disc.

3-1-6. Disc Judgment

The presence of a disk is judged from the spindle motor spinning start-up time.
Also, the disc size (12cm or 8cm) is judged from the spindle motor speed-up time and disc data.

3-2. Servo Operation at DVD Play

3-2-1. Optical Pickup Control

(1) DVD focus servo

The focus error signal output from the optical pickup for DVD (hereinafter referred to as optical pickup) is entered to the TK-47 board IC006: SSI33P3720A A to D (⑩ to ⑦P).

The balance amount and offset amount of the focus error signal is set by IC805 (CPU) via IC804 of the MB-78 board using the internal register of IC006.
The focus error signal is generated at TK-47 board IC006, amplified, and output from the FE terminal (㊴p).
The IC006 FOCUS error (DVD FE) signal is input to the MB-78 board via the flexible flat cable.
The error signal is switched according to whether the disc type is DVD or CD by the switch IC452, its signal level is adjusted by IC503 (OP amplifier ⑧, ⑨, ⑩p), and it is input to the servo DSP IC506 (CXD8730R) ㉖p.

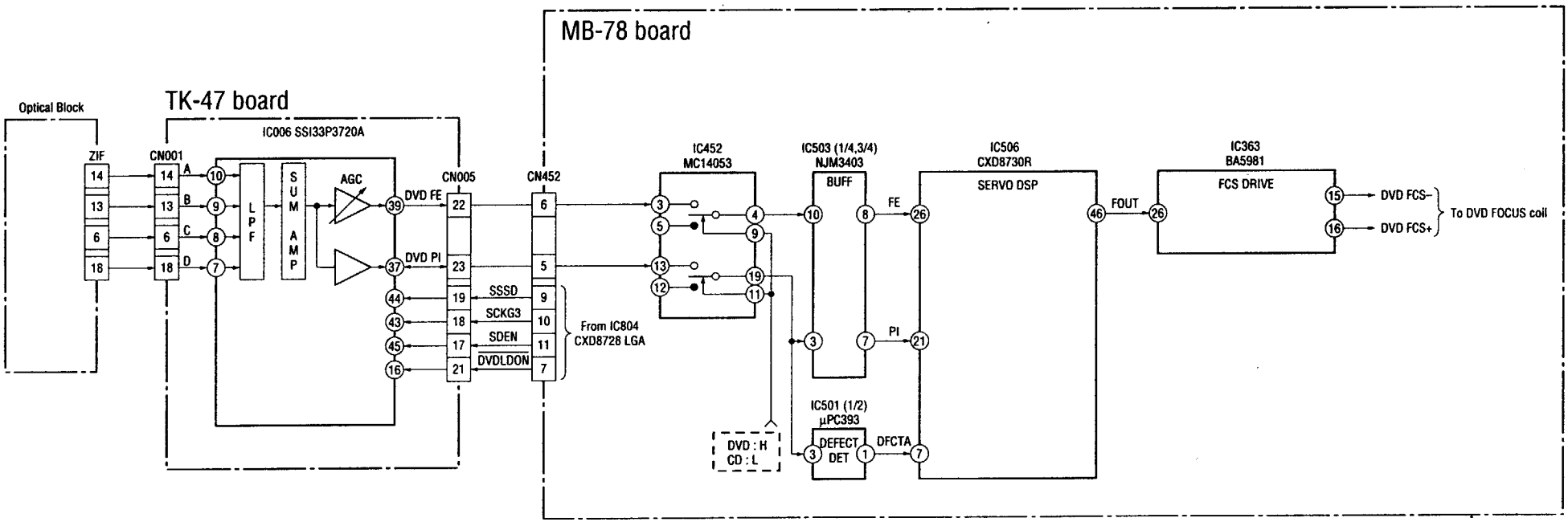


Figure 3-1. DVD focus servo, drive

The IC506 Servo DSP: CXD8730 on MB-78 board provides the following control in the focus servo system.

(a) Focus search

The optical pickup lens is moved toward a disc to turn on the focus servo.
The focus servo loop is turned on when the PI (Pull IN) signal (used for FOK: Focus OK) exceeds the specification (Vc +0.25V) and the FE signal zero-crossing is detected.

(b) Focus gain adjustment

The gain of digital filter in the IC506 is automatically adjusted so that the focus servo loop gain becomes optimum.
Consequently, the optimum gain for each disc to be played can be attained, besides correction of gain variations in focus actuator (coil) and optical pickup sensor (photodiode for focusing).

(c) Focus bias adjustment

The focus bias is added to the focus servo filter so as to minimize the jitter.
Consequently, a variation of optical pickup and disc can be automatically corrected.

(d) Focus jump

Operation carried out when playing back the DVD dual layer disc to perform focusing jump between layer 0 (PU side layer) and layer 1 (far end layer).
First the servo loop is turned off, the kick voltage is supplied to the focus actuator, and the focus is jumped to the targeted layer. As the focus approaches the desired layer, the FE signal appears. The voltage of this signal is monitored, the deceleration pulse is generated, and the focus servo is turned ON again after focusing.
These operations from the start to end of jumping are all performed inside the DSP.

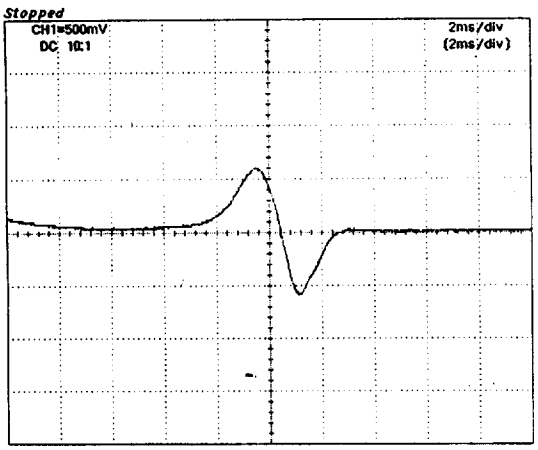


Figure 3-2. Example of S-shape waveform for the DVD disc (single layer) MB-78 board CN303 ③P

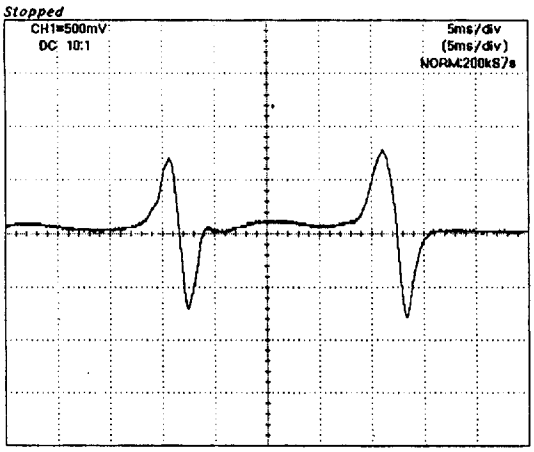


Figure 3-3. Example of S-shape waveform for the DVD disc (dual layer) MB-78 board CN303 ③P

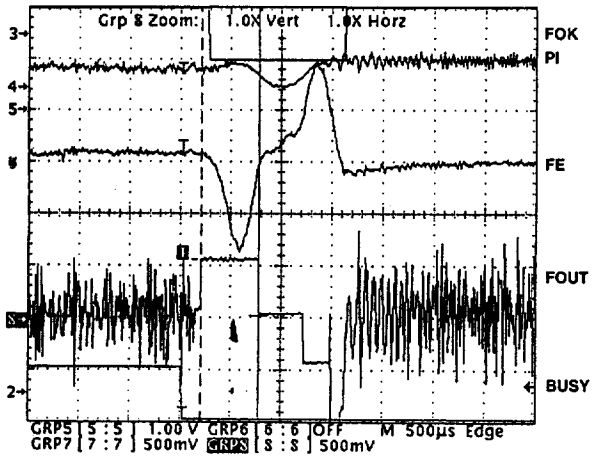


Figure 3-4. Focus jump waveform

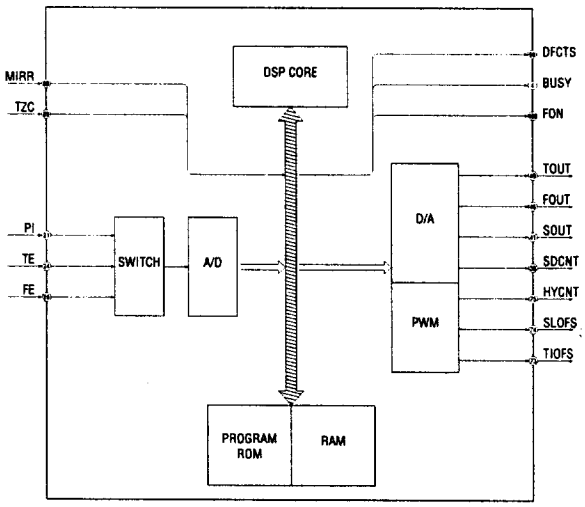


Figure 3-5. Example of S-shape waveform for MB-78 board CXD8730R (Layer) MB-78 board CN303 ③P

The FE signal input to IC506 (DSP CXD8730R) is low frequency boosted and gain-adjusted at the internal digital filter, and then output from the DSP as the focus drive signal (F OUT ㊻P) by the D/A converter inside the DSP.

The FOUT signal is input to the focus actuator (coil) drive IC (IC363:BA5981).

In IC363, voltage amplification, voltage conversion, and

current amplification are carried out to drive the focus actuator (coil) using the output signals of IC363 (DVD FCS+, DVD FCS-).

(2) DVD tracking servo

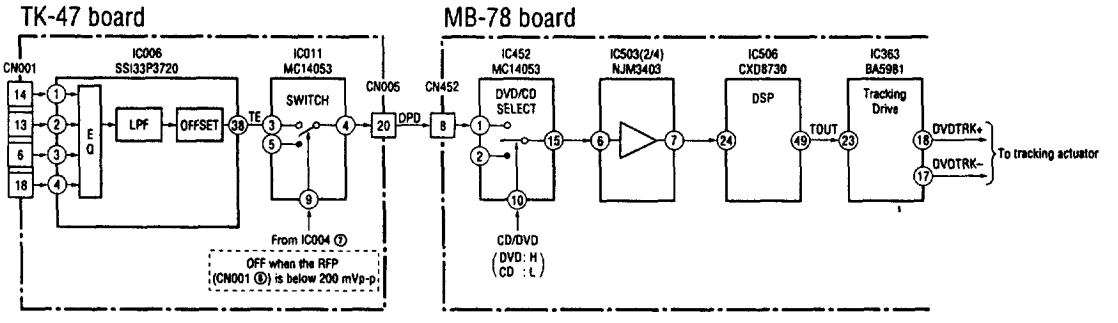


Figure. 3-6 DVD Tracking servo, drive

The tracking error signal output from optical pickup is entered to the IC006: SSI33P3720 A2 to D2 (① to ④P) on the TK-47 board. The tracking error signal is detected in the DPD (Differential Phase Detection) method.

The amplification degree and offset value of tracking error signal are set by internal register in the IC006.

The tracking error signal TE (IC006, ㊳P) is output from IC006, then it is entered to the switch IC (IC011: MC14053).

The switch IC shuts off tracking error signal when DVD RF signal (RFP) is below about 200mVp-p (AC component).

Tracking Error (TE) signal (DPD signal: Differential Phase Detection signal) generated in the IC006 is entered to the MB-78 board through a flexible flat cable.

TE (Tracking Error) signal passes through the switch IC, IC452 (MC14053 that switches CD tracking error and DVD tracking error (DPD) signal), and it is amplified at IC503 (NJM3403), then entered to the TE (㉔P) of IC506 (DSP: CXD8730R).

The Servo DSP IC provides the following control in the tracking servo system.

(a) Tracking gain adjustment

The gain of internal digital filter of IC is automatically adjusted so that the tracking servo loop gain becomes optimum.

Consequently, the optimum gain for each disc to be played can be attained, besides correction of gain variations in tracking actuator (coil) and optical pickup sensor (photodiode for tracking and focusing).

(b) Tracking jump control

At one track jump or N track jump (jumping many tracks) in asearching, generation of tracking pulses, control of tracking brake, and measurement of tracking jumps are executed.

The TE (Tracking Error) signal input to IC506 (Servo DSP CXD8730R) is low frequency boosted, high frequency phase compensated, and gain adjusted by the internal digital filter, and output from DSP by the DSP internal D/A converter as the tracking drive signal (T OUT ㊾P).

The T OUT signal is input to the IC (IC363:BA5981) for driving the tracking actuator (coil).

In IC363, voltage amplification, voltage conversion, and current amplification are carried out to BTL drive the tracking actuator (coil) using the output signals of IC363 (DVD TRK + ⑰P, DVD TRK – ⑱P).

The tracking zero-cross timing is generated by IC501 (μPC393) and IC508 (NJM3404).

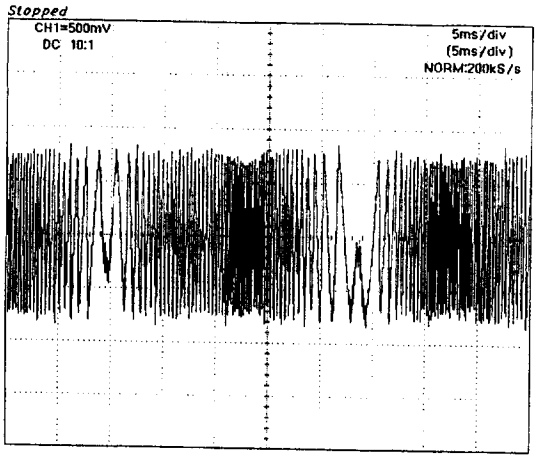


Figure 3-7. Trv (TE at tracking servo OFF) waveform at DVD disc, IC506㉔P

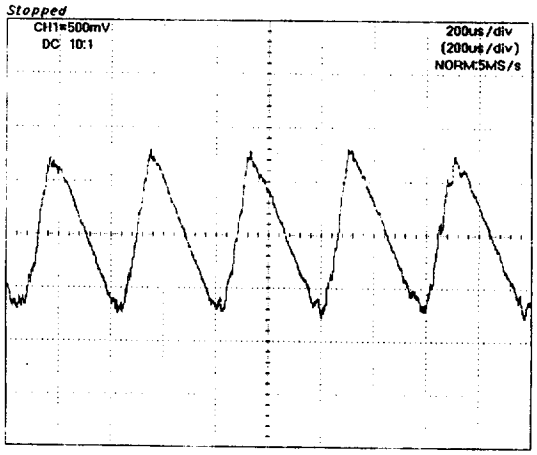


Figure 3-8. TE (enlarged Trv) waveform at DVD disc, IC506㉔P

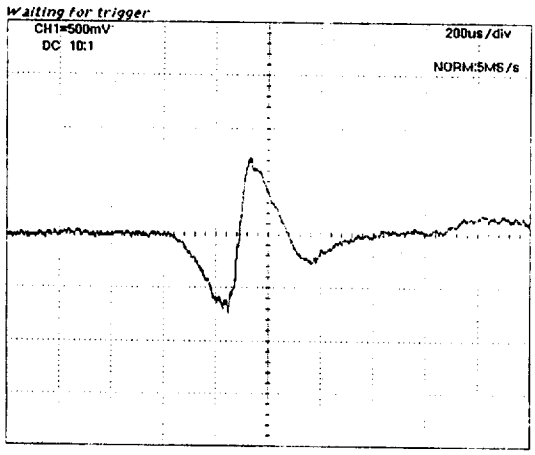


Figure 3-9. 1TJ (track jump) waveform at DVD disc, IC506㉔P

3-2-2. Sled control

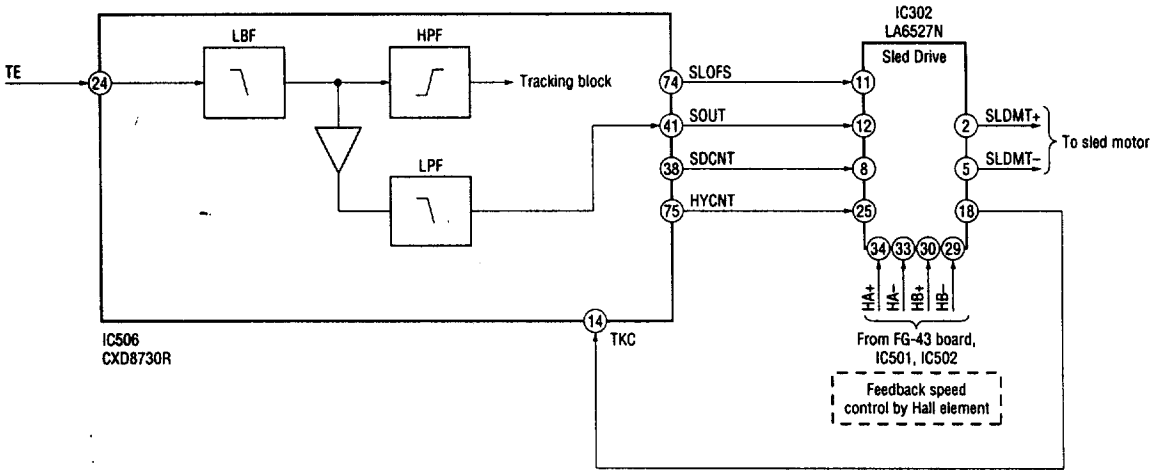


Figure 3-10. DVD Sled control

(1) Sled control during playing

During disc playing, namely, when the focus servo and tracking servo are turned on, the sled servo controls the sled motor so that an objective lens of optical pickup positions always in the center of movable range of tracking actuator.

The error signal of the sled servo is obtained by amplifying the low frequency components of TE by the digital filter in the DSP. Consequently, it cannot be observed externally. The error signal generated internally is output from SOUT (㊶P)) via the digital low pass filter, and input to the sled driver IC302 ⑫P).
The sled driver carries out sled speed control constantly, and adds the SOUT voltage to the control loop.

The Servo DSP IC506 CXD8730R carries out the following controls in the sled servo block.

(a) Sled error signal generation

Carries out tracking error TE processing to generate the sled error signal.

(b) Sled error amplification

Amplifies the sled error signal by the LPF (Low Pass Filter) composed of the digital filter and amplifier.

(c) Sled error ON/OFF

Turns ON the sled servo during normal playback, and turns it OFF when the tracking servo is OFF when playback starts, during search, etc.

The sled error signal is passed through the digital filter in IC506 (DSP), and output from the DSP as the SOUT (㊶P) signal from the D/A converter.

The SOUT signal is input to DVI (⑫P) of the sled drive IC (IC302:LA6527N).

The sled drive IC incorporates a speed (motor rotation speed) feed back control using the Hall element.
There are two speed detection Hall elements (HA, HB). The detection output is obtained from the sled motor board (FG-43 board) as the differential output of (HA+, HA–) (HB+, HB–).
The sled drive IC detects the inclination of the Hall element output waveform during sled motor rotation (differential value near the zero cross) to form the speed feedback.
In the sled drive IC, after the sled error signal is converted to the sled motor rotation speed signal, the voltage and current are amplified, and the sled (d.c.) motor is driven by the output signal (SLDMT+ ②P, SLDMT– ⑤P).

(2) Sled forced operation control

When driving the sled motor in operations other than playback, in other words during direct search, the sled speed target signal is input from IC506 (DSP:CXD8730R) ㊳P SDCNT to the sled motor driver IC302 (LA6527N) ⑧P. The data to IC506 (Servo DSP) is sent from the IC805 SH microcomputer.
The IC506 SLOFS ㊹P is the offset adjustment signal of IC302. It is used to adjust the voltage supplied between the motor terminals to 0 when the sled motor is stopping.

3-2-3. Spindle Control

This section describes the flow of control signals in the spindle servo during DVD playback.

The CLV control signal is generated from the RF signal obtained from the optical pickup in IC806 (CXD1865) to generate the two servo error signals-disc CLV speed error (MDSO ㊽ P) and CLV phase error (MDPO ㊼P).

These two error signals is added by IC301 (NJM3404) and output from ⑦P.

The spindle error output signal SPERR of the ⑦P of IC301 is input to the spindle drive IC (IC303:LB1896).

The IC303 is a 3-phase brushless motor drive IC, and it contains a spindle error signal amplifying circuit, gain switching circuit, and motor forced acceleration and deceleration control circuit.

Gain switching is done with the SPGC1 signal (⑪P).

Disc size (CD/DVD)	SPGC1 level
12 cm	H
8 cm	L

At the start and stop of disc playing, the forced acceleration and deceleration control is executed.

Control mode	Input signals	
	SPCTRL0 (⑨P)	SPCTRL1 (⑧P)
Acceleration	H	L
Deceleration	H	H
No control	L	H

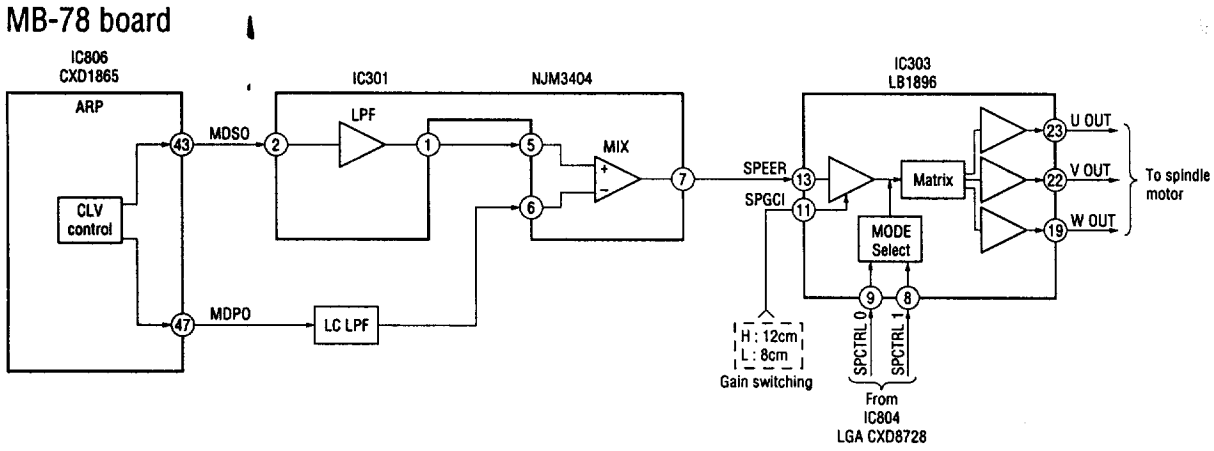


Figure 3-11. DVD spindle control

3-2-4. Tilt Control

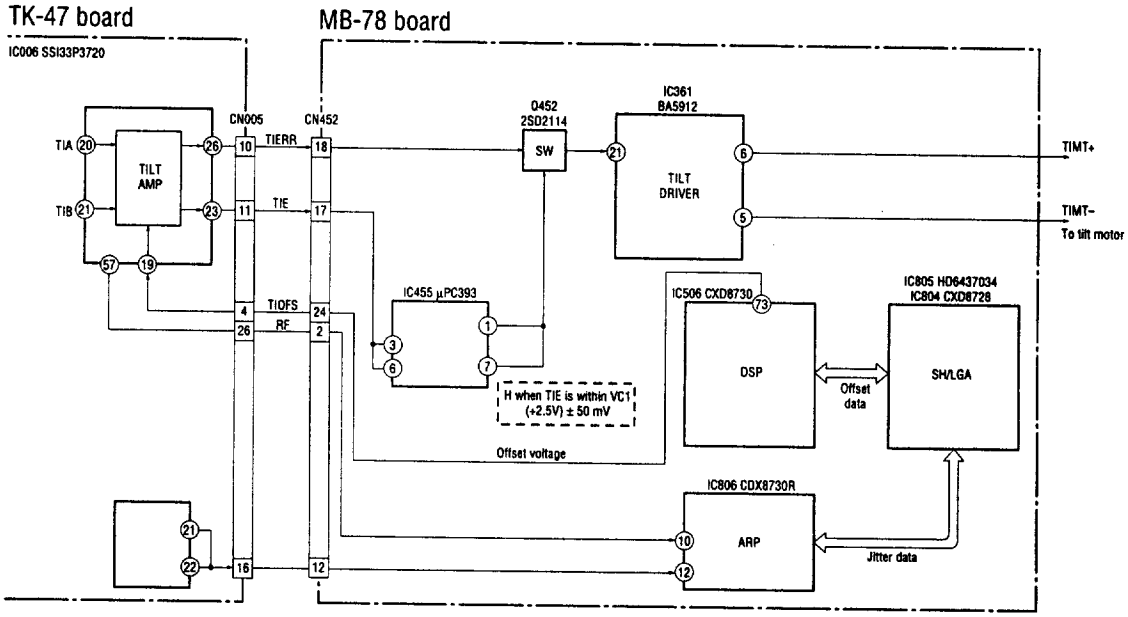


Figure. 3-12. Tilt control

(1) Tilt servo by tilt sensor

Tilt control using the tilt sensor of the optical pickup is performed at the start of DVD playback and CD playback.

The tilt sensor output signal of the optical pickup (TK-47 board CN001, ㊶P SKEW IN (TIA), ㊷P SKEW OUT (TIB)) is input to tilt amplifier (⑳, ㉑P) of IC006 (SS13P3720). After integration and amplification, it is output as the tilt error signal (TIERR ㉖P).

The servo on/off of the tilt error signal (TIERR) is controlled by the transistor SWQ452 of the MB-78 board.

When the tilt error signal (TIE) level drops within the specified value VCI (+2.5V) ±50 mV, the window comparator output TILTIN (①P or ⑦P) signal of IC455 (comparator μPC393) becomes the H level, and switch Q452 is controlled to switch to the ㉑P voltage level VC (+2.5V) of IC361.

As a result, the tilt servo goes OFF to form a dead band.

The TIERR signal during ON is input to the tilt drive IC361 (BA5912AFP).

In IC361, voltage amplification, voltage conversion, and current amplification is carried out, and the tilt motor (DC brush motor) is BTL-driven by the output signal (TIMT+⑥P, TIMT- ⑤P) of IC361.

(2) Tilt offset adjustment minimizing jitter

To optimize RF during DVD playback (excluding search), the jitter (JITTER:time-axis fluctuation of the RF signal) is measured, offset is added to the tilt servo loop, and the jitter is minimized.

As jitter is adjusted at shipment, normally this adjustment is not required during playback. However if the jitter deviates with time, the adjustment value may not be optimum according to the disc. In such cases, the jitter is measured prior to playback, and if it is deviated from the specified value, adjustments are started automatically.

The jitter value is measured by IC806 (CXD1865R) and the measured data is sent to the system controller IC805 (HD6437034) to determine the offset amount. The offset is voltage-generated by the PWM output of IC506 (DSP), and input to SSI33P3720 ⑲P as the offset voltage (TIOFS).

By performing the above three types of IC control, the jitter is adjusted to optimum.

3-3. Servo Operation at CD and Video CD Playing

3-3-1. Optical Pickup Control

(1) CD focus servo

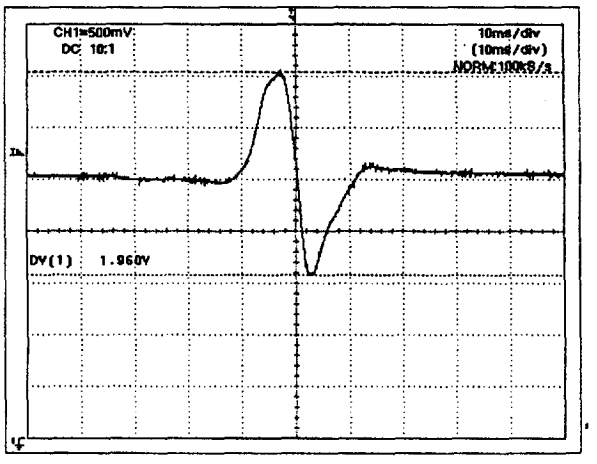


Figure 3-13. S waveform at CD disc (focus error), IC506㉖P

The RF signal (PDI, PD2) output from the CD optical pickup is converted to the focus error signal (CDFE, ⑮P) in IC005 (CD RF amplifier CXA2555Q) of the TK-47 board. The CD focus error signal (CDFE) is passed through the flexible flat cable and input to the switch IC452 (MC14053) of the MB-78 board. During CD playback, it is passed through the switch IC452, BuFF IC503, and input to ㉖P FE of IC506 (DSP:CXD8730R). The focus error signal is gain-adjusted, focus bias adjusted as done during DVD playback in the DSP.

The focus drive signal (FOUT, ㊻P) output from the DSP IC is input to the focus drive IC (IC363 BA5981FP) as done during DVD playback.

IC363 is a 4ch driver IC, but performs coil driving of each pickup by switching the level (H/L) of the MUTE terminal (⑨, ⑳P) during CD and DVD playback.

Play mode	MUTE signal	
	⑨P	⑳P
DVD	"H"	"L"
CD, Video CD	"L"	"H"

The IC363 amplifies voltage, transforms voltage, and amplifies current, then BLT drives the focus coil of CD pickup with its output signals (CD FCS+, CD FCS–).

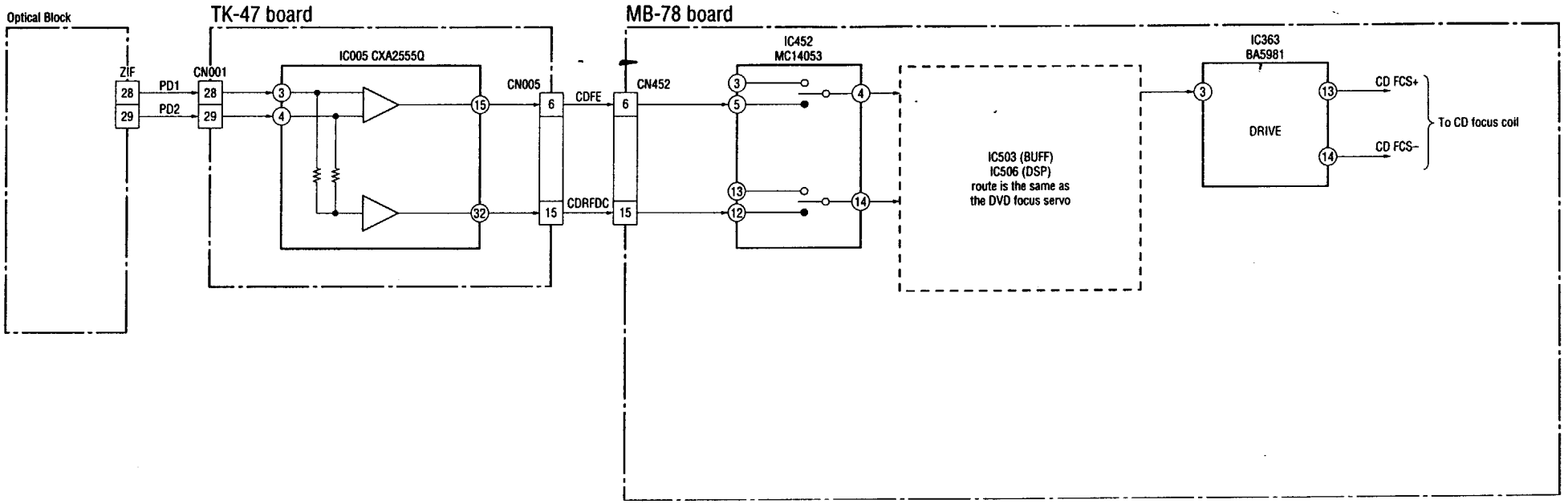


Figure. 3-14. CD focus servo, drive

(2) CD tracking servo

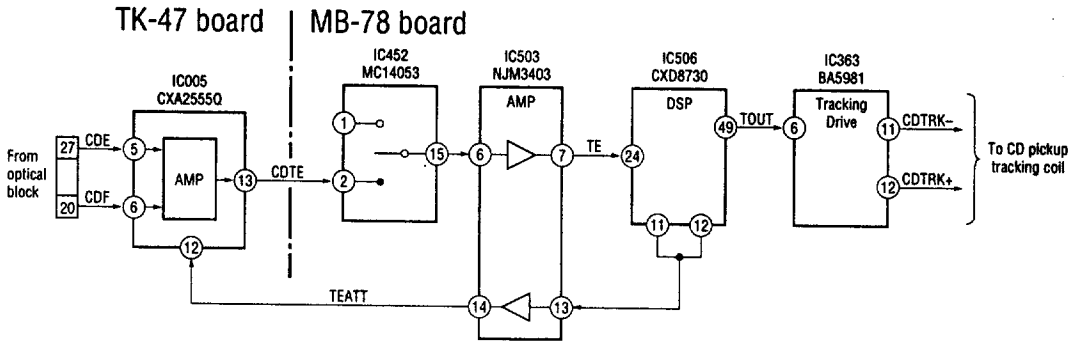


Figure 3-15. CD tracking servo

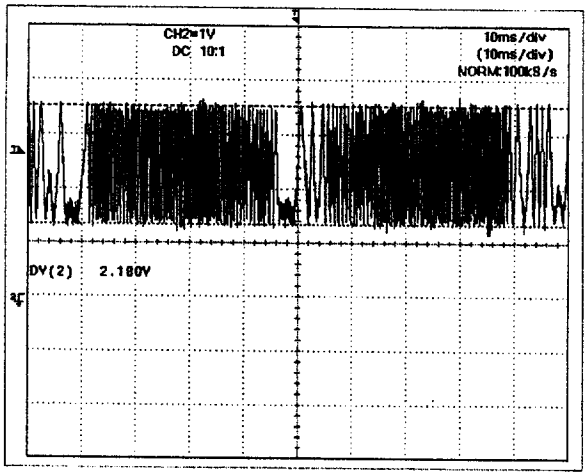


Figure 3-16. Trv (TE at tracking servo OFF) waveform at CD disc, IC506㉔P

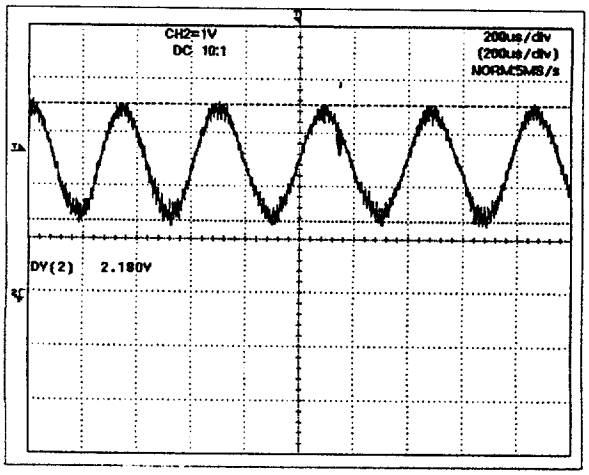


Figure 3-17. TE (enlarged Trv) waveform at CD disc, IC506㉔P

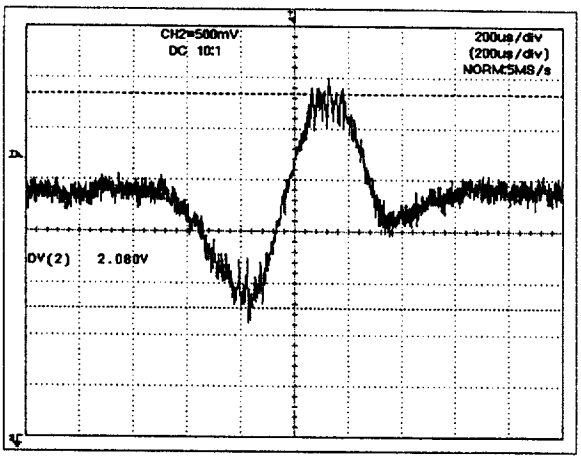


Figure 3-18. 1TJ (track jump) waveform at CD disc, IC506㉔P

The CDE and CDF signals output from the CD optical pickup are converted to the CD tracking error signal (CDTE ⑬P) at IC005 of (CXA2555Q) the TK-47 board.
The CDTE signal is input to the switch IC (IC452, MC14053) of the MB-78 board. During CD playback, it is passed through the switch IC (IC452), amplified at IC503, and input to ㉔P TE of IC506 (DSP CXD8730R).
Like DVD playback, the tracking error signal is gain-adjusted, tracking bias-adjusted, and tracking auto level-adjusted in the DSP.
The DSP tracking drive signal (T OUT ㊾P) is voltage-amplified, voltage-converted, and current-amplified by the IC (IC363 BA5981) for tracking driving, and used to drive the CD pickup tracking coil.
Track jump control during CD search is carried out by IC506 (DSP CXD8730R) as done during DVD search.
As a result, when performing 1 track jump or N track jump (many track jumps), tracking pulses are generated, the tracking zero cross timing is detected, tracking brake is controlled, and the number of track jumps is measured.

* Tracking auto level adjustment.
  This function operates only during CD and V-CD playback. When the TE level (traverse waveform) is small due to the inconsistency of the disc, this level adjustment is performed to eliminate the inconsistencies. Consequently, like gain adjustment, the adjustment is performed each time the disc is replaced (tray is opened), to set the traverse level to 2.0 Vp-p.

After setting the disc and turning ON the focus servo, the peak-to-peak value of the TE signal (this TE signal is called the traverse signal) is measured by the IC506 (DSP:CXD8730R).
The measurement results are read by the IC805 (system control IC) to determine the gain variable amount. The response (variable amount) is then returned again to IC506 (DSP:CXD8730R).
Upon receiving this, IC506 outputs control signal for the tracking auto level adjustment from ⑪P and ⑫P of the IC506 (DSP:CXD8730R). It is added by IC503 and converted to the analog voltage (TEATT signal).
The TEATT signal is input to ⑫P of IC005 (CXA2555) of the
TK-47 board, and gain-controlled inside the IC. The variable width is about ±3.0 dB.

3-3-2. CD Sled Control

CD sled control is exactly the same as the DVD.

However settings in IC506 (DSP:CXD8730R) differ.

3-3-3. CD Spindle Control

As the RF signal is processed inside IC806 (CXD1865), the process from the ARP is the same as the DVD.

3-3-4. Tilt Control

At CD playing, the tilt control is made using the tilt sensor of optical pickup in a period from the start of play (start of spindle rotation) to the completion of TOC data reading.

The tilt control in this case is same as tilt servo control by tilt sensor during DVD playing.

The tilt servo is turned off after the completion of TOC data reading.

The tilt servo mode ON/OFF control is done with the tilt servo amplifier in the IC006 (SSI33P3720) on the TK-47 board. (Figure. 3-12)

3-4. Disc Loading and Chucking

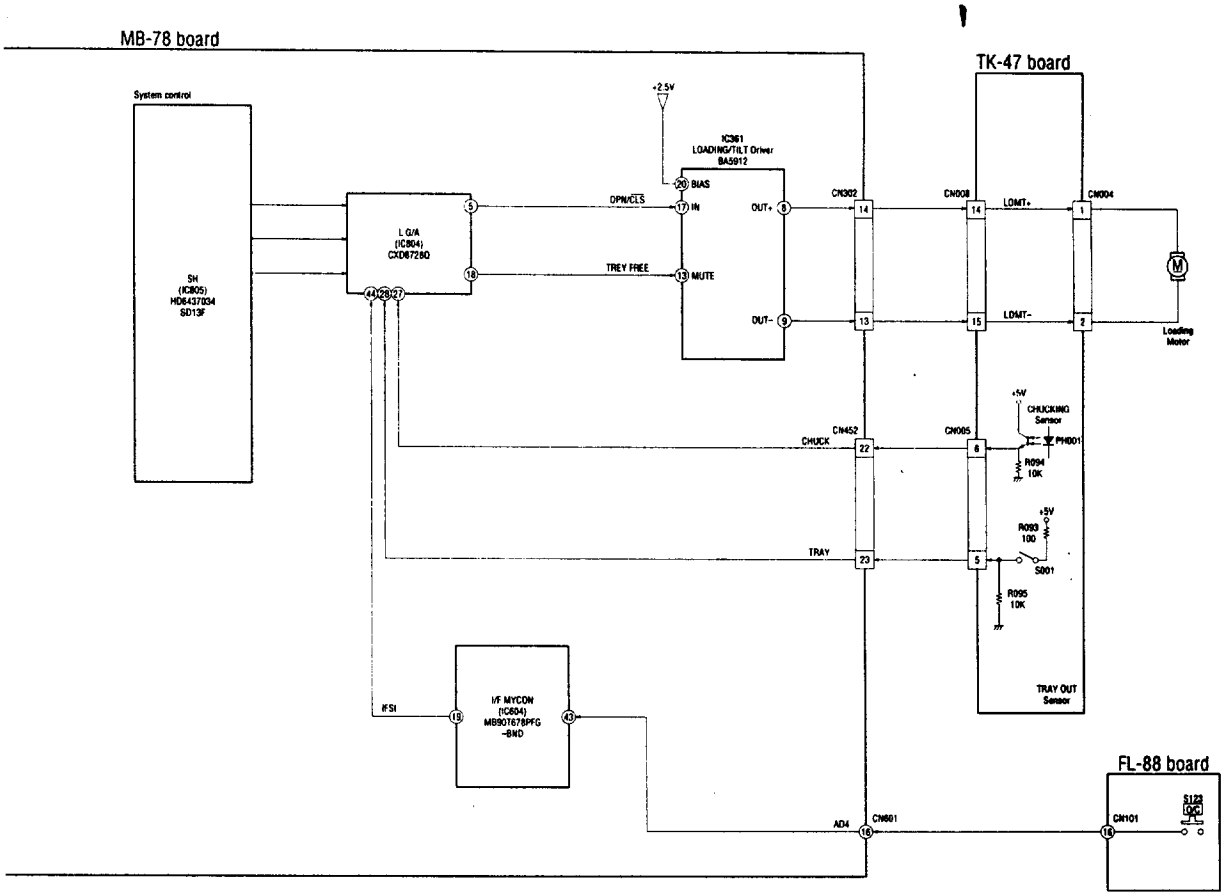


Figure. 3-19 Loading block

Disc loading, unloading, and chucking operations are performed with one DC motor. Its block diagram is dhown in Figure 3-19.

3-4-1. Motor Driver

The system controller IC (IC805) controls the open and close of the tray. It monitors the sensors of the mechanism and

controls the operations of the tray motor via the L G/A IC (IC804).

The tray open/close signal is output by 3-state PWM modulation from IC804.

H (5V) = Open

High Z = Stop

L (Gnd) = Close

The tray speed is controlled by increasing/decreasing the PWM duty ratio.

The TRAY FREE signal is used to control the Mute terminal of the driver directly, turn OFF the motor drive, and free the operations.

During the stop state, the potential difference between the two terminals of the motor is controlled to 0V, while during the Tray Free state, the motor is not controlled at all.

3-4-2. Tray Position Detection

Tray position detection is carried out by the chucking sensor PH001 and tray out sensor S001 on the TK-47 board. These signals are input to the MB-78 board via the flexible flat cable, and input to L G/A (IC804) CHUCK ㉗P, and TRAY ㉘P.

The relation between tray position and sensor signals is as shown below:

Mode	<TRAY OUT (CN005⑤)>	<CHUCKING (CN005⑥)>
Tray out position	H	L
Tray operating	L	L
Chucking position	L	H

3-5. Differentiation of Disc Type

This series can determine three types of discs (CD/DVD-SL/DVD-DL) at one time when performing focus-search.

3-5-1. CD/DVD Differentiation

The pit shape and track pitch are quite different between CD and DVD. Because of this difference, TE is not generated even if a large laser spot for CD is shot at a high density disk such as DVD. This feature is utilized to judge CD or DVD.

Specifically, even if DVD is played in the CD mode (the optical pickup operates at the CD side), TE is not generated almost all.

On the other hand, by playing CDs in the CD mode, naturally, the 2Vp-p traverse waveform (approx.) will be measured. This is used for the detection.

3-5-2. SL/DL Differentiation

SL/DL is differentiated by the PI level.

3-5-3. Differentiation

1) The servo system mode is CD (MB-78 board: IC452 "⑨"P and "⑩" are "L")
2) PI mode is DVD (MB-78 board: IC452 ⑪P is "H")
3) Both lasers turn ON
4) The spindle turns ON
5) The sled is moved to the external circumference slow.
6) Both focus actuators are moved up and down.
7) The signal is measured.

IC506 DSP (CXD8730R)

- When the p-p value of the CD traverse waveform (24p) is measured, the PI level of the DVD is measured at the same time.

- IC805 SH (system controller) reads the TE and PI levels measured by the DSP to differentiate between CD/DVD-SL/DVD-DL.

- CD/DVD differentiation: TE is generated as a clear traverse waveform,
  CD/DVD differentiation: Judged as CD if TE is generated as a clear traverse waveform.

SL/DL differentiation: The PI level becomes SL>DL.

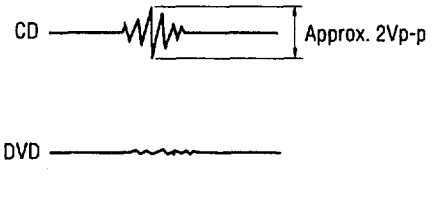


Figure. 3-20. Traverse waveform

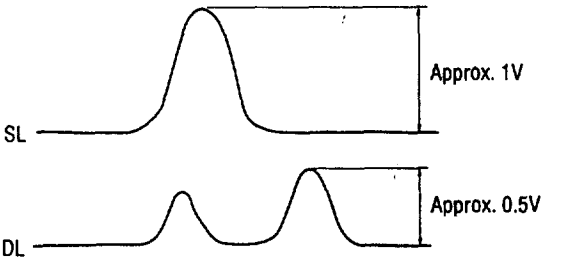
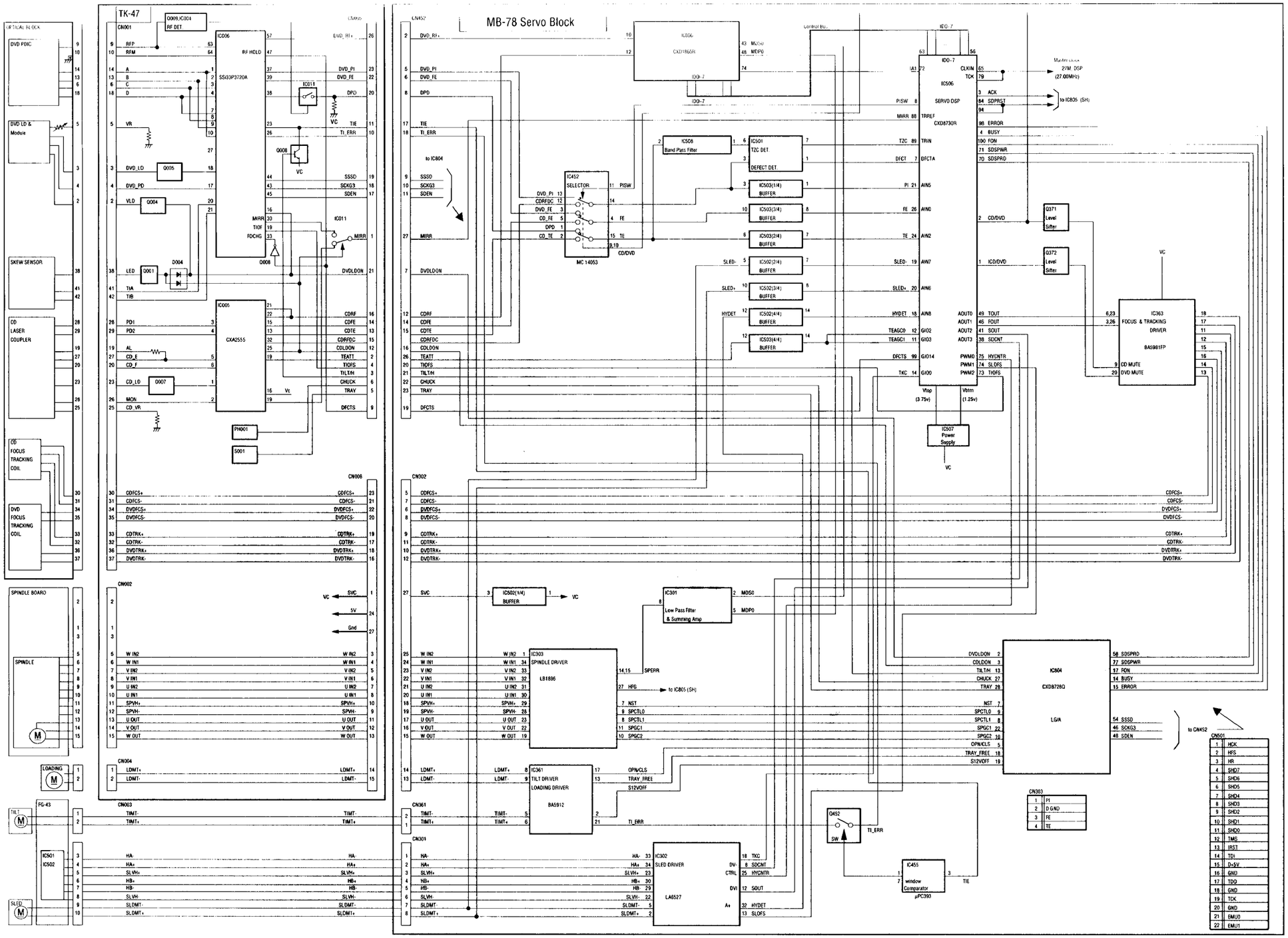


Figure. 3-21. PI waveform

3-6. Block diagram (Servo)

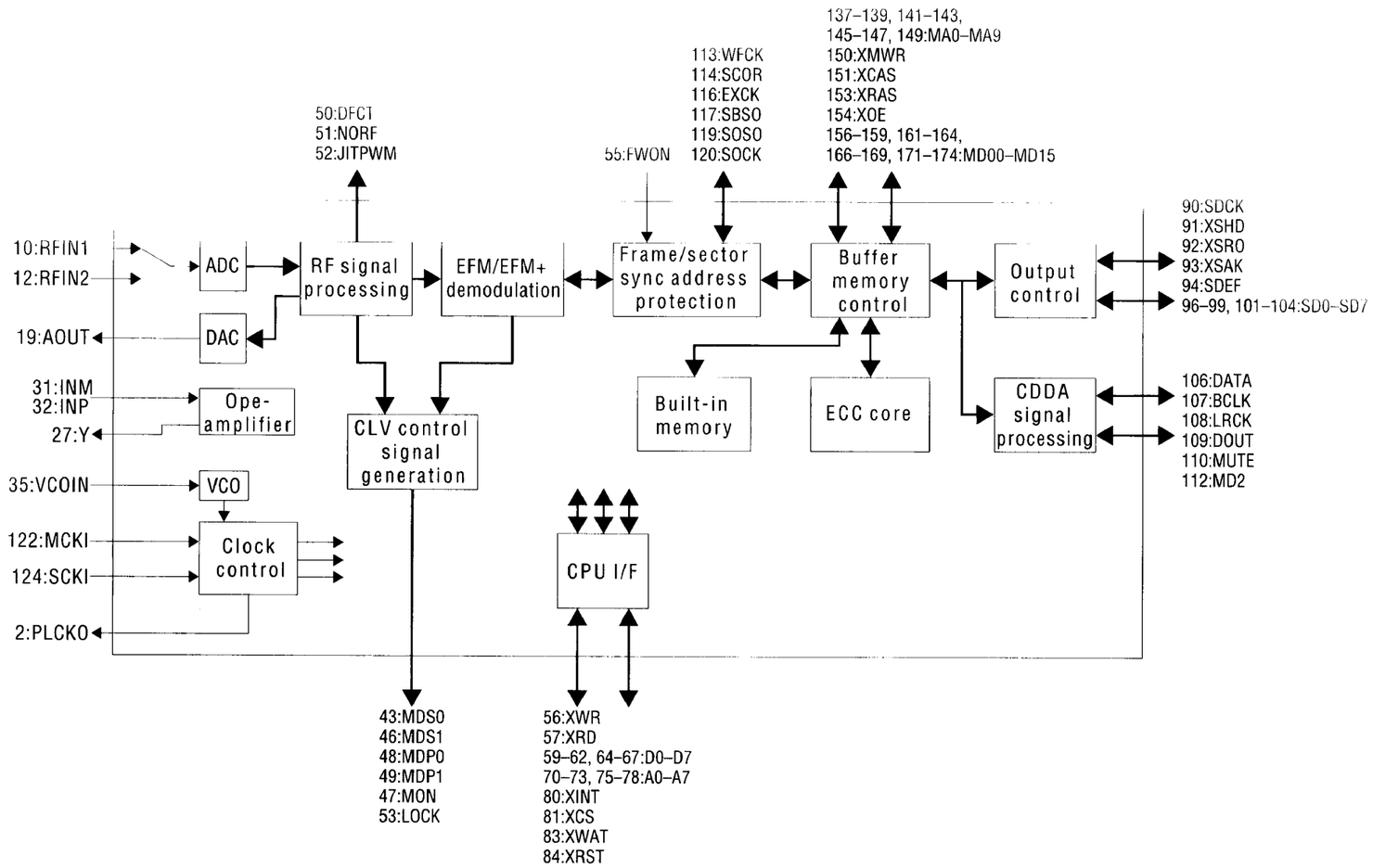


4. IC PIN DESCRIPTION

4-1. ARP

CXD1865R (IC806 on MB-78 board)

4-1-1. Block Diagram



4-1-2. Pin Functions

Pin No.	Signal Name	Direction	Level	Function
1	PLCKI	I	3.3	PLCK input
2	PLCKO	O	3.3	PLCK output
3	VSS	P		Digital ground
4	RFD	B	3.3	RF2 value data input/output
5	VDD	P	3.3	Digital positive power supply
6	VSS1	ADP		Digital ground
7	VRB	AI		ADC reference
8	VRBS	AI		ADC reference
9	GNDA1	AP		Analog ground
10	RFIN1	AI		RF input
11	AIN	AI		RF input
12	RFIN2	AI		RF input
13	VCCA1	AP	5	Analog positive power supply
14	VRTS	AI		ADC reference
15	VRT	AI		ADC reference
16	VDD1	ADP	5	Digital positive power supply
17	VSS2	ADP		Digital ground
18	VDD2	ADP	3.3	Digital positive power supply
19	AOUT	AO		DAC output
20	VCCA2	AP	3.3	Analog positive power supply
21	IREF	AI		DAC reference current
22	VREF	AI		DAC reference voltage
23	COMP	AI		DAC compensation pin
24	BIAS	AI		DAC bias pin
25	GNDA2	AP		Analog ground
26	VCCA3	AP	3.3	Analog positive power supply
27	Y	AO		Ope-amplifier output
28	FR1	AO		Feedback resistance switching 1
29	FR2	AO		Feedback resistance switching 2
30	FR3	AO		Feedback resistance switching 3
31	INM	AI		Ope-amplifier negative input
32	INP	AI		Ope-amplifier positive input
33	GNDA3	AP		Analog ground
34	GNDA4	AP		Analog ground
35	VCOIN	AI		VCC control input
36	R1	AI		VCO external resistor 1
37	R2	AI		VCO external resistor 2
38	TEST0	AO		VCO test output
39	VCCA4	AP		Analog positive power supply
40	VCK	B	3.3	VCO oscillation output/test input

Pin No.	Signal Name	Direction	Level	Function
41	VSS	P		Digital ground
42	TESTA	I	3.3	Test pin
43	MDSO	O	5	CLV speed error
44	VDD	P	3.3	Digital positive power supply
45	VSS	P		Digital ground
46	MDS1	O	5	CLV speed error
47	MON	O	5	Motor on
48	MDP0	O	5	CLV phase error
49	MDP1	O	5	CLV phase error
50	DFCT	O	5	Defect detection output
51	NORF	O	5	NO RF detection output
52	JITPWM	O	5	Jitter PWM output
53	LOCK	O	5	EFM lock output
54	VDDS	P		Digital positive power supply
55	FWON	I	5	Sync protection on
56	XWR	I	3.3	CPU write
57	XRD	I	3.3	CPU read
58	VDD	P	3.3	Digital positive power supply
59	D0	B	5	CPU data
60	D1	B	5	CPU data
61	D2	B	5	CPU data
62	D3	B	5	CPU data
63	VSS	P		Digital ground
64	D4	B	5	CPU data
65	D5	B	5	CPU data
66	D6	B	5	CPU data
67	D7	B	5	CPU data
68	VDDS	P	5	Digital positive power supply
69	TEST	I	5	Test pin
70	A0	I	5	CPU address
71	A1	I	5	CPU address
72	A2	I	5	CPU address
73	A3	I	5	CPU address
74	SCEN(!)	I	3.3	
75	A4	I	5	CPU address
76	A5	I	5	CPU address
77	A6	I	5	CPU address
78	A7	I	5	CPU address
79	VDD	P	3.3	Digital positive power supply
80	XINT	OD	5	Interruption
81	XCS	I	5	Chip select
82	VSS	P		Digital ground

Pin No.	Signal Name	Direction	Level	Function
83	XWAT	OD	5	Wait
84	XRST	I	5	Reset
85	VDD	P	3.3	Digital positive power supply
86	TEST0	I	3.3	Test pin
87	SCMD	I	3.3	Test pin
88	ETST	I	3.3	Test pin
89	VSS			Digital ground
90	SDCK	O	3.3	SD bus clock
91	XSHD	O	3.3	SD bus header
92	XSRQ	I	3.3	SD bus REQ
93	XSAK	O	3.3	SD bus ACK
94	SDEF	O	3.3	SD bus error flag
95	VDD	P	3.3	Digital positive power supply
96	SD0	O (B)	3.3	SD bus data
97	SD1	O (B)	3.3	SD bus data
98	SD2	O (B)	3.3	SD bus data
99	SD3	O (B)	3.3	SD bus data
100	VSS	P		Digital ground
101	SD4	O (B)	3.3	SD bus data
102	SD5	O (B)	3.3	SD bus data
103	SD6	O (B)	3.3	SD bus data
104	SD7	O (B)	3.3	SD bus data
105	VDD	P	3.3	Digital positive power supply
106	DATA	O	3.3	CDDA data
107	BCLK	O	3.3	CDDA bit clock
108	LRCK	O	3.3	CDDA LR clock
109	DOUT	O	3.3	Digital out
110	MUTE	I	5	Audio mute
111	VSS	P		Digital ground
112	MD2	I	5	Digital out on
113	WFCK	O	5	Frame clock
114	SCOR	O	5	Subcode sync
115	VDDS	P	5	Digital positive power supply
116	EXCK	I	5	SBSO reading clock
117	SBSO	O	5	SubP to W serial output
118	VSS	P		Digital ground
119	SQSO	O	5	SubQ serial output
120	SQCK	I	5	SBSO reading clock
121	VSS	P		Digital ground
122	MCKI	I	5	ECC clock
123	VDDS	P	5	Digital positive power supply
124	SCKI	I	5	System clock

Pin No.	Signal Name	Direction	Level	Function
125	VSS	P		Digital ground
126	MNT0	B	3.3	Monitor bus
127	MNT1	B	3.3	Monitor bus
128	MNT2	B	3.3	Monitor bus
129	MNT3	B	3.3	Monitor bus
130	VDD	P	3.3	Digital positive power supply
131	MNT4	B	3.3	Monitor bus
132	MNT5	B	3.3	Monitor bus
133	MNT6	B	3.3	Monitor bus
134	MNT7	B	3.3	Monitor bus
135	ESTB	O	3.3	Error information strobe
136	VSS	P		Digital ground
137	MA0	O	3.3	DRAM address
138	MA1	O	3.3	DRAM address
139	MA2	O	3.3	DRAM address
140	VDD	P	3.3	Digital positive power supply
141	MA3	O	3.3	DRAM address
142	MA4	O	3.3	DRAM address
143	MA5	O	3.3	DRAM address
144	VSS	P		Digital ground
145	MA6	O	3.3	DRAM address
146	MA7	O	3.3	DRAM address
147	MA8	O	3.3	DRAM address
148	VDD	P	3.3	Digital positive power supply
149	MA9	O	3.3	DRAM address
150	XMWR	O	3.3	DRAM write enable
151	XCAS	O	3.3	DRAM CAS
152	VSS	P		Digital ground
153	XRAS	O	3.3	DRAM RAS
154	XOE	O	3.3	DRAM output enable
155	VDD	P	3.3	Digital positive power supply
156	MD00	B	3.3	DRAM data
157	MD01	B	3.3	DRAM data
158	MD02	B	3.3	DRAM data
159	MD03	B	3.3	DRAM data
160	VSS	P		Digital ground
161	MD04	B	3.3	DRAM data
162	MD05	B	3.3	DRAM data
163	MD06	B	3.3	DRAM data
164	MD07	B	3.3	DRAM data
165	VDD	P	3.3	Digital positive power supply
166	MD08	B	3.3	DRAM data

Pin No.	Signal Name	Direction	Level	Function
167	MD09	B	3.3	DRAM data
168	MD10	B	3.3	DRAM data
169	MD11	B	3.3	DRAM data
170	VSS	P		Digital ground
171	MD12	B	3.3	DRAM data
172	MD13	B	3.3	DRAM data
173	MD14	B	3.3	DRAM data
174	MD15	B	3.3	DRAM data
175	PLDIR	I	3.3	PLCK direction control
176	VSS	P		Digital ground

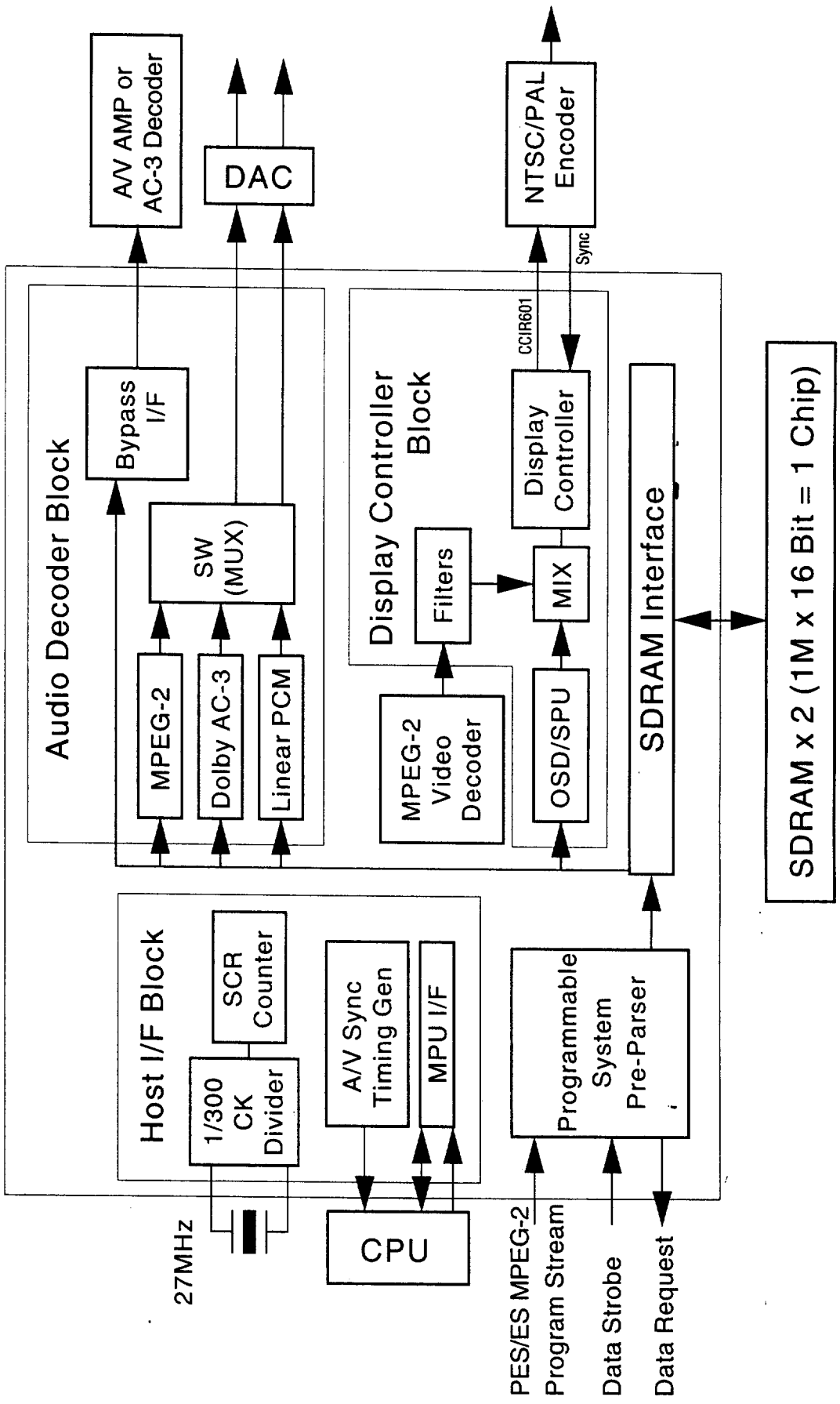
*Function of direction

I [input], O [output], OD [output (open drain)], O(B) [output (bi-direction during test)], B[input/output (bi-direction)], P [power supply], ADP [power supply (digital for analog cell)], AP [power supply (analog)].

AI [input (analog)], AO [output (analog)]

4-2. AV Decoder L64020 (MB-78 Board IC203)

4-2-1. Block Diagram



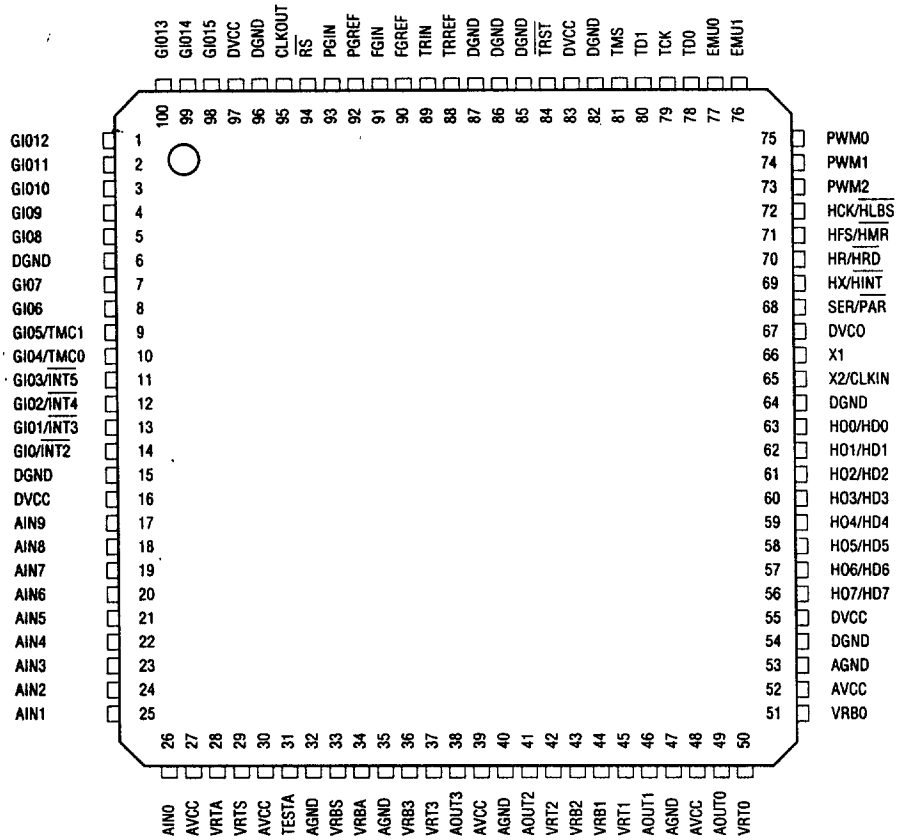
4-2-2. Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name	Pin No..	Signal Name
1	VSS	41	NC	80	NC
2	SBD_7	42	VDD	81	VSS
3	SBD_6	43	A_2	82	PD_5
4	SBD_5	44	A_1	83	PD_6
5	SBD_4	45	A_0	84	PD_7
6	VDD	46	VSS	85	VSS
7	SBD_3	47	D_7	86	BLANK
8	SBD_2	48	D_6	87	CREF
9	SBD_1	49	D_5	88	EXT_OSD_0
10	SBD_0	50	D_4	89	EXT_OSD_1
11	VSS	51	D_3	90	EXT_OSD_2
12	CH_DATA_0	52	D-2	91	EXT_OSD_3
13	CH_DATA_1	53	D-1	92	NC
14	CH_DATA_2	54	D-0	93	VDD
15	CH_DATA_3	55	VSS	94	ACLK_441
16	CH_DATA_4	56	SYSCLK	95	ACLK_48
17	CH_DATA_5	57	RESET_N	96	ACLK_32
18	CH_DATA_6	58	DREQ_N	97	VSS
19	CH_DATA_7	59	INTR_N	98	CD_BLK
20	VSS	60	BUSMODE	99	CD_LRCLK
21	TOS_N	61	VDD	100	CD_ALCK
22	NC	62	DTACK_N/	101	CD_ASDATA
23	NC		RDY_N	102	SPDIF_N
24	ERROR_N	63	READ/READ_N	103	A_ACLK
25	VDD	64	DS_N/WRITE_N	104	VDD
26	AVALID_N	65	WAIT_N/WTN	105	BCLK
27	VVALID_N	66	VSS	106	LRCLK
28	DCK	67	AS_N	107	ASDATA
29	VREQ_N	68	CS_N	108	NC
30	AREQ_N	69	VS	109	NC
31	NC	70	HS	110	VSS
32	NC	71	VDD	111	SPDIF_OUT
33	VSS	72	OSD_ACTIVE	112	AUDIO_SYNC
34	A_8	73	PD_0	113	TM1
35	A_7	74	PD_1	114	TM0
36	A_6	75	VSS	115	ZTEST
37	A_5	76	PD_2	116	SCAN_TE
38	A_4	77	PD_3	117	PREQ_N
39	A_3	78	PD_4	118	VDD
40	VDD	79	VDD	119	SBC_15

Pin No.	Signal Name
120	SBD14
121	NC
122	SBD_13
123	VSS
124	SBD_12
125	SBD_11
126	SBD_10
127	VDD
128	SBD_9
129	SBD_8
130	SCLK
131	VSS
132	SBA_9
133	SBA_8
134	SBA_7
135	VDD
136	SBA_6
137	SBA_5
138	SBA_4
139	VSS
140	SBA_3
141	SBA_2
142	SBA_1
143	VDD
144	SBA_0
145	SBA_10
146	SBA_11
147	VSS
148	SCSI_N
149	SCS_N
150	SRAS_N
151	VDD
152	SRAS_N
153	SWE_N
154	SDQM
155	VSS
156	PLLVDD
157	NC
158	PLLVSS
159	VDD
160	NC

4-3. Digital Signal Processor CXD8730R (MB-78 Board IC506)

4-3-1. Pin Assignment



4-3-2. Pin Functions

This section describes signals. The input/output states of signals are differentiated by the input (I), output (O), and high impedance (Z). Each signal is grouped by function.

Pin	Signal Name	I/O	Type	Function
Analog signal pin				
29	VRTS	O	Analog	AD upper limit reference voltage output. When using 3.75V for the upper limit reference voltage, connect the VRTS output to the VRTA input.
28	VRTA	I	Analog	AD upper limit reference voltage input.
33	VRBS	O	Analog	AD lower limit reference voltage output. When using 1.25V for the lower limit reference voltage, connect the VRBS output to the VRBA input.
34	VRBA	I	Analog	AD lower limit reference voltage input.
26-27	AIN0-AIN9	I	Analog	Analog data input signal. Analog signal input to the 8-bit AD converter. The input to the AD converter is switched automatically by the analog switch.
49	AOUT0	O	Analog	DAC0 buffer output signal. DAC0 buffer output. The power down mode can be selected.
50	VRT0	I	Analog	DAC0 buffer upper limit reference voltage input.
51	VRB0	I	Analog	DAC0 buffer lower limit reference voltage input.
46	AOUT1	O	Analog	DAC1 buffer output signal. DAC1 buffer output. The power down mode can be selected.
45	VRT1	I	Analog	DAC1 buffer upper limit reference voltage input.
44	VRB1	I	Analog	DAC1 buffer lower limit reference voltage input.
41	AOUT2	O	Analog	DAC2 buffer output signal. DAC2 buffer output. The power down mode can be selected.
42	VRT2	I	Analog	DAC1 buffer upper limit reference voltage input.
43	VRB2	I	Analog	DAC2 buffer upper limit reference voltage input.
38	AOUT3	O	Analog	DAC3 buffer output signal. DAC3 buffer output. The power down mode can be selected.
37	VRT3	I	Analog	DAC2 buffer upper limit reference voltage input.
36	VRB3	I	Analog	DAC3 buffer lower limit reference voltage input.
PWM pin				
75-73	PWM0-PWM2	O	CMOS	PWM output signal. 8-bit PWM output. The output pulse width can be set any value.
Host interface pin				
68	SER/$\overline{\text{PAR}}$	I	TTL	Host interface serial/parallel mode selection. H:Serial, L:Parallel.
70	HR/$\overline{\text{HWR}}$	I	TTL (Internal pull-up)	Host serial data/host data read strobe signal input. In the serial mode, the serial data is input. In the parallel mode, the data read strobe signal is input.

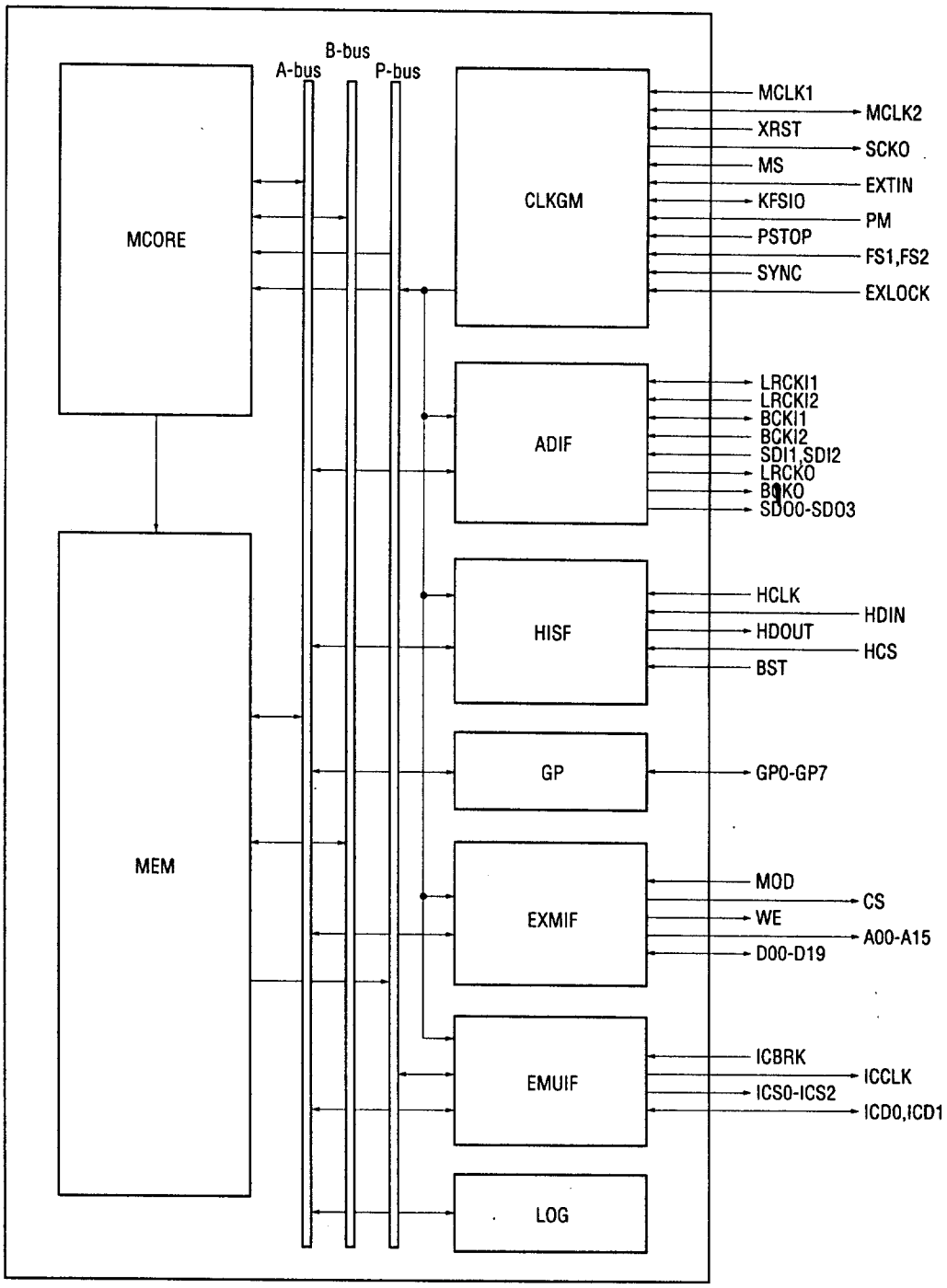
Pin	Signal Name	I/O	Type	Function
71	HFS/$\overline{HWR}$	I	TTL	Frame sync signal/host data write strobe signal input for data transmission. In the serial mode, the data transmission frame sync signal is input. In the parallel mode, the data write strobe signal is input.
69	HX/$\overline{HINT}$	O/Z	CMOS	Host serial data/host interrupt signal output. In the serial mode, the serial data is output. In the parallel mode, the host interrupt signal is output.
72	HCK/$\overline{HLBS}$	I	TTL	Clock/host low byte select signal input for host serial data transmission. In the serial mode, the serial data transmission clock is input. In the parallel mode, the low byte select signal is input.
63-57	HO0/HD0-HO6/HD6	I/O	TTL	General data output/parallel data input/output. In the serial mode, the general data is output. In the parallel mode, the parallel data is input/output.
56	HIO/HD7	I/O	TTL	General data/parallel data input/output. In the serial mode, the general data is input/output. In the parallel mode, the low byte select signal is input.
General input/output pin				
14	GIO0/$\overline{INT2}$	I/O	TTL	General data input/output/$\overline{INT2}$ external interrupt signal input. Selected by the interrupt control register.
13	GIO1/$\overline{INT3}$	I/O	TTL	General data input/output/$\overline{INT3}$ external interrupt signal input. Selected by the interrupt control register.
12	GIO2/$\overline{INT4}$	I/O	TTL	General data input/output/$\overline{INT4}$ external interrupt signal input. Selected by the interrupt control register.
11	GIO3/$\overline{INT5}$	I/O	TTL	General data input/output/$\overline{INT5}$ external interrupt signal input. Selected by the interrupt control register.
10	GIO4/TMC0	I/O	TTL	General data input/output/timer 0 external clock input. Selected by the timer control register.
9	GIO5/TMC1	I/O	TTL	General data input/output/timer 1 external clock input. Selected by the timer control register.
8, 7, 5-1, 100-98	GIO6-GIO15	I/O	TTL	General data input/output. The input/output is set by the GIO control register. The input data is set to the general input register. The data of the general output register is output. When using a GIO from GIO0 to GIO5 as the interrupt signal or input clock, be careful not to set the corresponding control bit to the output when changing the value of the GIO control register value.
Track counter				
88	TTREF	I	TTL (Hysteresis)	Track counter reference pulse signal input.
89	TRIN	I	TTL (Hysteresis)	Track pulse signal input.

Pin	Signal Name	I/O	Type	Function
FG/PG counter				
90	FGREF	I	TTL (Hysteresis)	FG counter reference pulse signal input. The polarity of the input can also be checked by the host output register (bit 10).
91	FGIN	I	TTL (Hysteresis)	FG pulse signal input. The polarity of the input can also be checked by the host output register (bit 9).
92	PGREF	I	TTL (Hysteresis)	PG counter reference pulse signal input.
93	PGIN	I	TTL (Hysteresis)	PG pulse signal input.
JTAG pin				
77	EMU0	I/O/Z	TTL (Internal pull-up)	Emulator pin 0
76	EMU1	I/O/Z	TTL (Internal pull-up)	Emulator pin 1
84	$\overline{\text{TRST}}$	I	TTL (Internal pull-up)	JTAG test reset pin
81	TMS	I	TTL (Internal pull-up)	JTAG test mode select pin
78	TDO	O/Z	TTL	JTAG test data output pin
80	TDI	I	TTL (Internal pull-up)	JTAG test data input pin
79	TCK	I/O	TTL (Internal pull-up)	JTAG test clock
Other signal pins				
95	CLKOUT1	O	COMS	Master clock output signal
94	$\overline{\text{RS}}$	I	TTL (Internal pull-up)	Reset input
65	X2/CLKIN	I	Oscillator	Internal oscillator input/clock input
66	X1	O	Oscillator	Internal oscillator output
31	TESTA	O	–	Reserved pin. Use without connecting.
Power supply pin				
16, 55, 67, 83, 97	DVcc	–	–	+5V supply pin for digital circuit.
6, 15, 54, 64, 82, 85-87, 96	DGNO	–	–	Ground pin for digital circuit.

Pin	Signal Name	I/O	Type	Function
27, 30, 39, 48, 52	AVcc	–	–	+5V supply pin for analog circuit.
32, 35, 40, 47, 53	AGND	–	–	Ground for analog circuit.

4-4. AC3 Decoder
MB86342 (MB-78 Board IC104)

4-4-1. Block Diagram

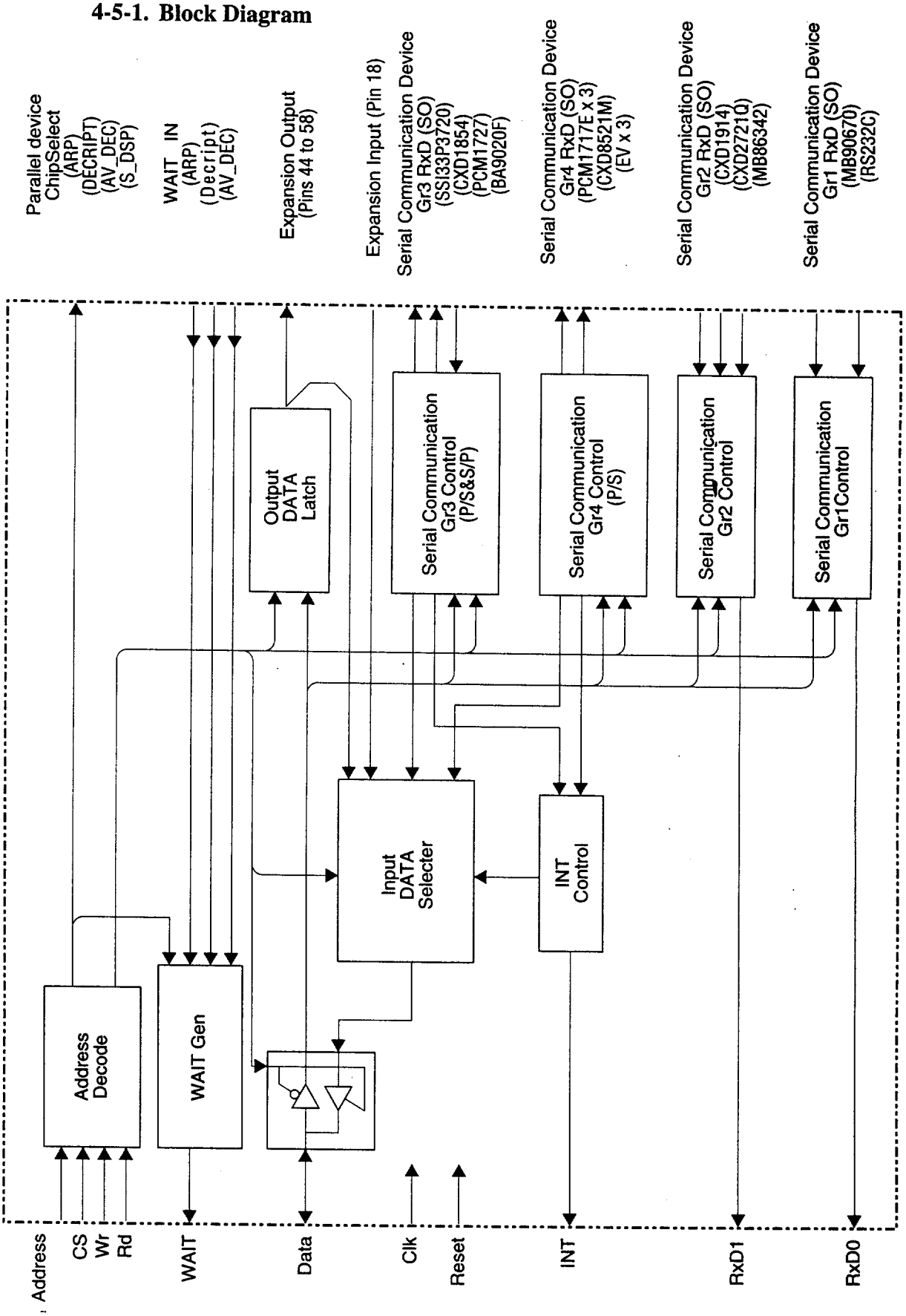


4-4-2. Pin Functions

Pin No.	Signal Name	I/O	Function
5	MCLKI	I	Clock input pin
6	MCLK2	I/O	Clock input/output pin
1	XRST	I	Reset signal input
8	SCKO	O	System clock output pin
12	MS	I	Master/slave selection pin L:Master (Crystal oscillation) H:Slave (External clock)
16	SYNC	I	Sync/async selection pin (L:Sync, H:Async)
2	EXTIN	I	System clock (384 fs) input pin
13, 14	FS1, FS2	I	Sampling frequency switching signal input pin
7	KFSIO	I/O	Audio clock (384 fs) input/output pin
9	PM	I	Test pin (normally set to GND.)
10	PSTOP	I	PLL/crystal oscillator control signal input pin
11	EXLOCK	I	Lock signal input pin
41	HCLK	I	Host interface clock input pin
43	HDIN	I	Host interface serial data input pin
44	HDOUT	O	Host interface serial data output pin
42	HCS	I	Host interface chip select input pin
45	BST	I	Normally fixed at "L".
39-35, 32-30	GP0-GP7	I/O	8-bit general port input/output pin
17	LRCKI1	I/O	Sampling clock input/output pin for audio interface serial data
18	BCKI1	I/O	Bit clock input/output pin for audio interface serial data
20	LRCKI2	I	Sampling clock input pin for audio interface serial data
21	BCK12	I	Bit clock input pin for audio interface serial data
19, 22	SDI1, SDI2	I	Serial data input pin for audio interface
23	LRCKO	O	Sampling clock output pin for audio interface serial data
24	BCKO	O	Bit clock output pin for audio interface serial data
25-27	SDO1-SDO3	O	Serial data output pin for audio interface
46	MOD	I	Pass mode control signal input pin
47	CS	O	Chip select output pin for external SRAM interface
48	WE	O	Write enable output pin for external SRAM interface
67-66, 64-55, 52-49	A00-A15	O	Serial data output pin for external SRAM interface
92, 91, 89-85 82-80, 77-68	D00-D19	I/O	Data input/output pin for external SRAM interface
93	ICCLK	O	Clock output pin for emulator
94	ICBRK	I	External brake control signal input pin for emulator
96, 95	ICD0, ICD1	I/O	Data/address input/output pin for emulator
99-97	ICS0-ICS2	O	Status output pin for emulator

4-5. Large Gate Array CXD8728 (MB-78 Board IC804)

4-5-1. Block Diagram



4-5-2. Pin Functions

Pin No.	Signal Name	RD/WR,SHIF	Function
1	VDD		VDD
2	DVDLDONn	I/O, RD/WR	DVD laser light/off signal:ON when "L"
3	CDLDONn	I/O, RD/WR	CD laser light/off signal:ON when "L"
4	CD/DVD	I/O, RD/WR	Signal differentiating between CD and DVD:DVD when "H".
5	OPN/CLS	I/O, RD/WR	Tray open/close. Open at "H" and Close at "L". Stop when "Hiz".
6	DRERR	I/O, RD	DIR LC89051V error signal. Error when "H".
7	NSTn	I/O, RD/WR	Spindle motor non-control voltage input. Stop when set to 0V.
8	SPCTL1	I/O, RD/WR	Switches the spindle servo operation mode. Can be set to control, non-control, acceleration.
9	SPCTL0	I/O, RD/WR	Switches the operation mode between SPCTL1 and 2Bit. Can be set to control, non-control, acceleration.
10	SPGC2	I/O, RD/WR	Spindle servo gain control signal. Switches the gain of the "post stage" amplifier.
11	DETON (T_out)	I/O, RD/WR	CD/DVD differentiation sensor ON/OFF SW signal:ON when "H" (Data output during memory test)
12	ACDDET	I/O, RD	CD/DVD differentiation signal (sensor output which is waveform-shaped)
13	TILT/H	I/O, RD/WR	TILT servo characteristics switching signal
14	BUSY2	I/O, RD	Servo DSP busy flag:Busy when "L"
15	ERROR (T_IN)	I/O, RD	Servo DSP error flag:Error when "L" (clk signal input during the memory test)
16	LOCK	I/O, RD	From ARP
17	FOK	I/O, RD	From DSP
18	TRAYFREE	I/O, RD/WR	Releases the tray driver. Open when "L".
19	S12VOFF	I/O, RD/WR	Servo 12V power supply OFF. 12V on when "H"
20	VDD		VDD
21	GND		GND
22	SPGC1	I/O, RD/WR	Spindle servo gain control signal. Switches the gain of the "first stage" amplifier.
23	TBLR	I/O, RD/WR	Changer roulette rotation. Rotates when "H".
24	TBLL	I/O, RD/WR	Changer roulette rotation. Rotates when "H".
25	LDOUTn	I/O, RD/WR	Changer loading OUT. Loading out when "L".
26	LDINn	I/O, RD/WR	Changer loading IN. Loading in when "L".
27	ACHUCK	I/O, RD	Mechanism chucking detection signal. "H" when chucking.
28	ATRAY	I/O, RD	Tray open signal. "H" when the tray is open.

Pin No.	Signal Name	RD/WR,SHIF	Function
29	TSENS	I/O, RD	Changer roulette position detection sensor. No groove when "L". Groove is present when "H".
30	DSENS	I/O, RD	Changer disc presence detection sensor. Present when "H" and absent when "L".
31	S3	I/O, RD	DISC detection position (rotary sensor) 0 to 7 value
32	S2	I/O, RD	DISC detection position (rotary sensor) 0 to 7 value
33	S1	I/O, RD	DISC detection position (rotary sensor) 0 to 7 value
34	ACSn	I/O, RD/WR	AC3_DEC MB86432 chip select
35	ACSI	Serial I/F, IN	AC3_DEC MB86432 output data
36	VCSn	I/O, RD/WR	V_Enc CXD1914Q chip select (XVENCCS)
37	VSI	Serial I/F, IN	V_Enc CXD1914Q output data
38	KLTn	I/O, RD/WR	Karaoke DSP CXD2721Q serial data latch
39			
40	VDD		VDD
41	GND		GND
42	GND		GND
43	KSI	Serial I/F, IN	Karaoke DSP CXD2721Q output data
44	IFSI	Serial I/F, IN	IF CON output data
45	DBSI	Serial I/F, IN	Debug serial port output data
46	SCKG3	Serial I/F, OUT	Serial Group3 Clock
47	SOG3	Serial I/F, OUT	Serial group 3 output data
48	SDEN	I/O, RD/WR	SSI (SSI133P3720) chip select
49	DCSn	I/O, RD/WR	DNR (CXD1854Q) chip select (XDNRCS)
50	MLTn	I/O, RD/WR	DAC (CXD8696R) data latch (DACLT)
51	ECSn	I/O, RD/WR	EEPROM (BA9020F) chip select (XEERCS)
52	SSSD	Serial I/F, IN	SSI (SSI133P3720) input/output data
53	EESI	Serial I/F, IN	EEPROM (BA9020F) output data
54	EWCn	I/O, RD/WR	EEPROM (BA9020F) write control (XEEWE)
55	EBSYn	I/O, RD	EEPROM (BA9020F) BUSY signal (XEERBS)
56	IRDn	Peripheral I/F, OUT	Peripheral read signal
57	IWRn	Peripheral I/F, OUT	Peripheral write signal
58	SDSPRDn	Peripheral I/F, OUT	Servo DSP chip select & read
59	ARPCSn	Peripheral I/F, OUT	ARP chip select
60	ARPINT	Peripheral I/F, IN	ARP INT signal input
61	ARPWTn	Peripheral I/F, IN	ARP WAIT signal input
62	DCRCSn	Peripheral I/F, OUT	DECRYPT chip select
63	DCRINT	Peripheral I/F, IN	DECRYPT INT signal input
64	DCRWTn	Peripheral I/F, IN	DECRYPT WAIT signal input
65	AVCSn	Peripheral I/F, OUT	AV_DEC(L64020) Chip Select
66	AVWTn	Peripheral I/F, IN	AV_DEC (L64020) WAIT signal input. Masked by AVCSn.
67	XWAITn	SHIFT, OUT	
68	XIRQ3	SHIFT, OUT	

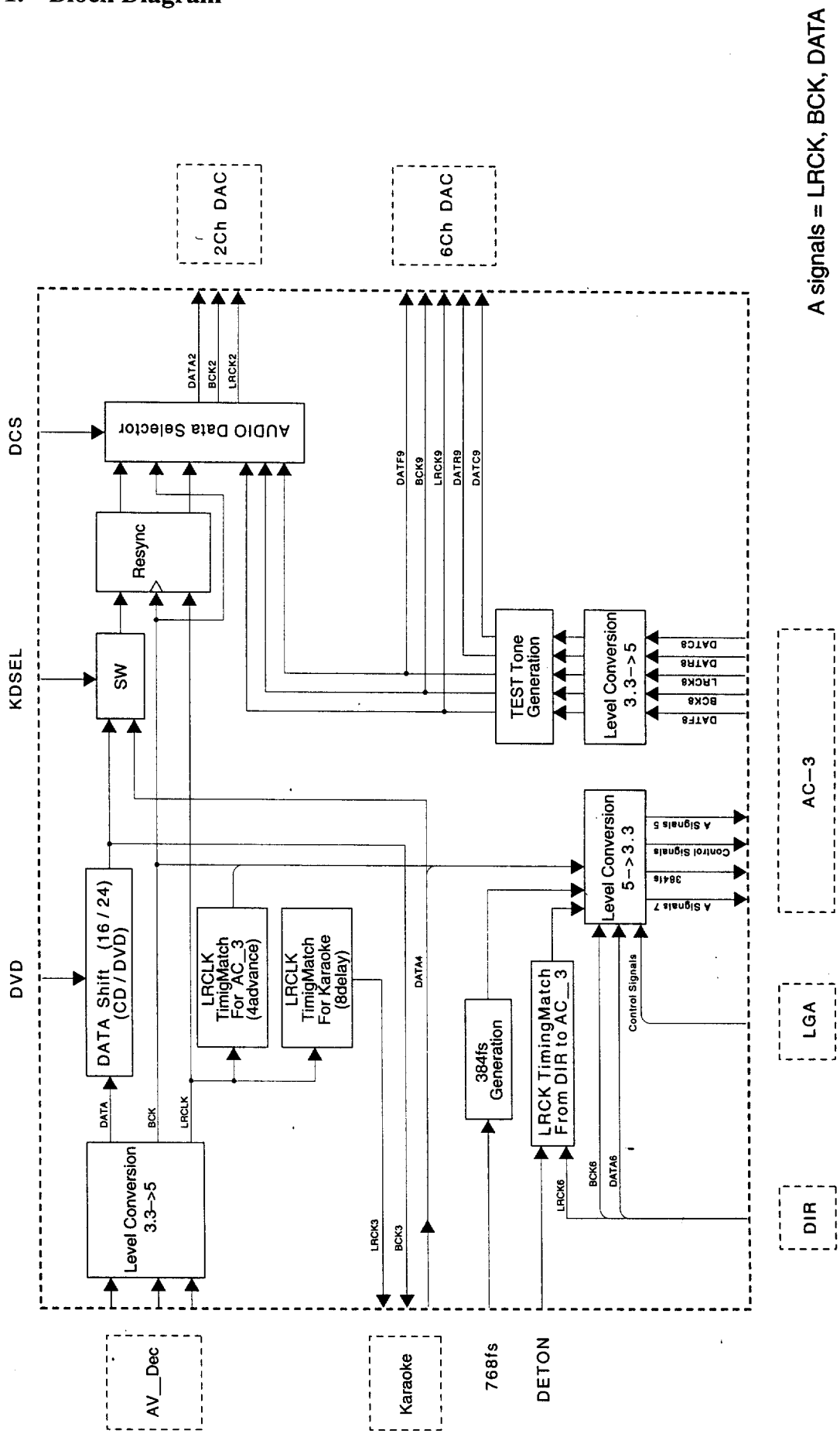
Pin No.	Signal Name	RD/WR,SHIF	Function
69	SIG1	SHIF, OUT	
70	SIG2	SHIF, OUT	
71	XIRQ7	SHIF, OUT	
72	XCS6n	SHIF, IN	
73	XRDn	SHIF, IN	
74	XLWRn	SHIF, IN	
75	HA21	SHIF, IN	
76	HA20	SHIF, IN	
77	SDSPWRn	Peripheral I/F, OUT	Servo DSP chip select & write
78	CPCK	SHIF, IN	CPU clock
79	GND		GND
80	GND		GND
81	VDD		VDD
82	BUSGATE	BUSCNT, OUT	BUS buffer control. Gate off when "H".
83	HA19	SHIF, IN	
84	HA7	SHIF, IN	
85	HA6	SHIF, IN	
86	HA5	SHIF, IN	
87	HA4	SHIF, IN	
88	HA3	SHIF, IN	
89	HA2	SHIF, IN	
90	HA1	SHIF, IN	
91	HA0	SHIF, IN	
92	HD7	SHIF, bidir	
93	HD6	SHIF, bidir	
94	HD5	SHIF, bidir	
95	HD4	SHIF, bidir	
96	HD3	SHIF, bidir	
97	HD2	SHIF, bidir	
98	HD1	SHIF, bidir	
99	HD0	SHIF, bidir	
100	VDD		VDD
101	GND		GND
102	FWON	I/O, RD/WR	ARP block, sync protection circuit ON/OFF (for external control)
103	MD2	I/O, RD/WR	ARP block, digital audio output mute.
104	MUTE	I/O, RD/WR	ARP block, audio output mute.
105	DFCT	I/O, RD/WR	ARP block, defect detection.
106	NORF	I/O, RD/WR	ARP block, No-RF detection
107	DBGINTn	SHI, IN	Serial IC interruption for debugging. Level
108	SOG1	Serial I/F, IN	Serial Group 1 (TXD)
109	IFSO	Serial I/F, OUT	TXD to Serial Group 1 IF
110	DBSO	Serial I/F, OUT	TxD to Serial Group 1 Diagnostic Connector

Pin No.	Signal Name	RD/WR,SHIF	Function
111	(DIAGN)	H/W, IN	
112	(CTS)	H/W, OUT	
113	SCKG2, (IRQ5)	H/W, IN/OUT	SH serial channel 1 SCLK (GROUP2) or IRQ5 output
114	AVCK	H/W, OUT	AV Enc CXD1914 serial clock
115	CK27M	H/W, IN	AV CK Resync 27Mclock
116	GAIN6n	I/O, RD/WR	AUDIO output gain switching signal 4 (AC-3) channel L, R (or spare port)
117	D2LTn	I/O, RD/WR	2 Channel DAC Latch
118	PDCLK	HW/IN	13.5 M CLOCK input
119			
120	VDD		VDD
121	GND		GND
122	GND		GND
123	RESETn	H/W, IN	System reset
124	CTS	I/O, RD/WR	Host status notification. Ready when "L"
125	DIAGN	I/O, RD/WR	Presence/absence of connector of diagnostic connector. Connected when "L".
126	TEB		Memory test setting. Normally pull up.
127	HSYNC	HW/IN	HSYNC input
128	SCKG2PS	H/W, OUT	Serial Group 2 sync clock (P/S) 1 MHz
129	SOG2PS	H/W, OUT	Serial Group2 TxD
130	DCÅl3D	I/O, RD/WR	DCS control
131	TON	I/O, RD/WR	Test tone
132	XIFBSY	I/O, RD	I/F CON BUSY Status
133	XSHINT	I/O, RD/WR	Communication request to I/F CON. Request for interrupt when "L"
134	SCKG4	Serial I/F, OUT	Serial Group 4 Clock
135	SOG4	Serial I/F, OUT	Serial group 4 output data
136	DDLT1n	I/O, RD/WR	DAC PCM1716 data latch-1 (L/R) Grp4
137	DDLT2n	I/O, RD/WR	DAC PCM1716 data latch-2 (SL/SR) Grp4
138	DDLT3n	I/O, RD/WR	DAC PCM1716 data latch-3 (C/SW) Grp4
139	DLTn	I/O, RD/WR	DIR LC89051V data latch Grp4
140	OHSYNC	H/W, OUT	Advance HSYNC output
141	TOFC1	I/O, RD/WR	Tracking Offset Control 1
142	TOFC2	I/O, RD/WR	Tracking Offset Control 2
143	SCKG4n	Serial I/F, OUT	DIR LC89051V serial clock
144	KADTSEL	I/O, RD/WR	Selects whether to use the Karaoke DSP CXD2721Q. When used=H (KD_SEL)
145	KRDY	I/O, RD	Selects whether to enable or disable Karaoke DSP CXD2721Q transmission. When transmission is enabled=H

Pin No.	Signal Name	RD/WR,SHIF	Function
146	CLAPBSY	I/O, RD	When the clap IC MSM6654 is generating sounds, outputs the "H" level. When the power is turned ON.
147	OTASUKE	I/O, RD	Active "L" level when the help IC NJM2072M is needed.
148	DVD/VTR	I/O, RD/WR	Video control. Selects the video signal external input. Selects the external input when "H" is output.
149	AVCNT	I/O, RD/WR	Video control. AV control signal. EURO AV ON when "H" is output.
150	EÅIV/Y	I/O, RD/WR	Video control. Composite, YC selection. YC is selected when "L" is output.
151	EÅIV/RGB	I/O, RD/WR	Video control. Composite, RGB selection. RGB is selected when "L" is output.
152	VS1	I/O, RD/WR	Video control. S pin control signal.
153	FS	I/O, RD/WR	Frequency setting:L=44.1 kHz, H=48 kHz
154	EXCLOCK	I/O, RD/WR	External frequency lock detection:L=Locked. H=Not locked.
155	BST	I/O, RD/WR	Boost strap (when boosting the farm) Set to the "H" level.
156	CLAPSW1	I/O, RD/WR	Phrase input corresponding to the sound generated by the clap IC MSM6654. (Required)
157	CLAPSW0	I/O, RD/WR	Phrase input corresponding to the sound generated by the clap IC MSM6654. (Required)
158	DOUTCTL	I/O, RD/WR	Digital out ON/OFF ("H":ON, "L":OFF) (DO-CTL)
159	GND		GND
160	GND		GND

4-6. Middle Gate Array CXD8746 (IC101 on MB-78 board)

4-6-1. Block Diagram



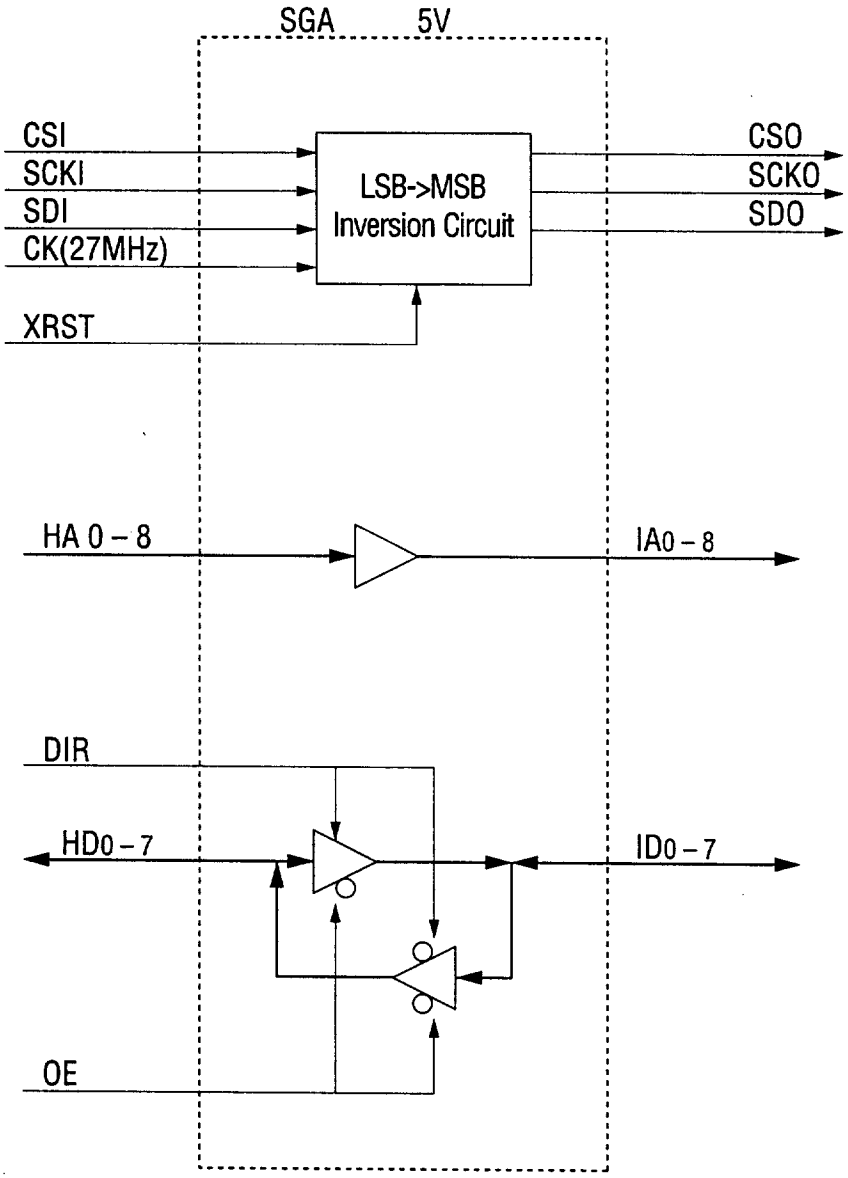
4-6-2. Pin Functions

Pin No.	Signal Name	I/O	Level	From/For	Function
1	ARSTI	IN	5V		
2	XLOCKI	IN	5V		
3	DVD	IN	5V		
4	SCK21	IN	5V	LGA	AC3 serial communication
5	SO21	IN	5V	LGA	AC3 serial communication
6	ACSI	IN	5V	LGA	AC3 serial communication
7	BSTI	IN	5V	LGA	
8					
9	FS768	IN	5V		768fs
10					
11	MCK27	IN	5V		27M clock
12					
13	TON	IN	5V		Test tone on/off
14	DC3D	IN	5V		2ch DAC data switching
15	DATA2	OUT	5V	2Ch DAC	Audio signal to 2ch DAC
16	LRCK2	OUT	5V	2Ch DAC	Audio signal to 2ch DAC
17	BCK2	OUT	5V	2Ch DAC	Audio signal to 2ch DAC
18					
19	BCK9	OUT	5V	6Ch DAC	Audio signal to 6ch DAC
20	LRCK9	OUT	5V	6Ch DAC	Audio signal to 6ch DAC
21	DATF9	OUT	5V	6Ch DAC	Audio signal to 6ch DAC
22	DATR9	OUT	5V	6Ch DAC	Audio signal to 6ch DAC
23	DATC9	OUT	5V	6Ch DAC	Audio signal to 6ch DAC
24					
25	BSTO	OUT	3.3V	AC-3	
26	ACSO	OUT	3.3V	AC-3	AC_3 serial communication
27	SO20	OUT	3.3V	AC-3	AC_3 serial communication
28	SCK20	OUT	3.3V	AC-3	AC_3 serial communication
29	DETON	IN	3.3V		
30	XLOCKO	OUT	3.3V	AC-3	
31	ARSTO	OUT	3.3V	AC-3	AC_3 reset signal
32					
33	DATC8	IN	3.3V	AC-3	Audio (C/S) signal from AC_3
34	DATR8	IN	3.3V	AC-3	Audio (RL/RR) signal from AC_3
35	DATF8	IN	3.3V	AC-3	Audio (FR/FL) signal from AC_3
36	BCK8	IN	3.3V	AC-3	Audio signal from AC_3
37	LRCK8	IN	3.3V	AC-3	Audio signal from AC_3
38					
39	DATA7	OUT	3.3V	AC-3	Audio signal (DIR) to AC_3
40	BCK7	OUT	3.3V	AC-3	Audio signal (DIR) to AC_3
41	LRCK7	OUT	3.3V	AC-3	Audio signal (DIR) to AC_3

Pin No.	Signal Name	I/O	Level	From/For	Function
42					
43	DATA5	OUT	3.3V	AC-3	Audio signal (Karaoke) to AC_3
44	BCK5	OUT	3.3V	AC-3	Audio signal (Karaoke) to AC_3
45	LRCK5	OUT	3.3V	AC-3	Audio signal (Karaoke) to AC_3
47	FS384	OUT	3.3V	AC-3	AC3 384fs
48					
49	LRCK3	OUT	5V	Karaoke	Audio signal to karaoke
50	BCK3	OUT	5V	Karaoke	Audio signal to karaoke
51	DATA3	OUT	5V	Karaoke	Audio signal to karaoke
52	DATA4	IN	5V	Karaoke	Audio signal from karaoke
53					
54	DATA1	IN	3.3V	AV-Dec	Audio signal from AV-Dec
55	LRCK1	IN	3.3V	AV-Dec	Audio signal from AV-Dec
56	BCK1	IN	3.3V	AV-Dec	Audio signal from AV-Dec
57					
58	DATA6	IN	5V	DIR	Audio signal from DIR
59	LRCK6	IN	5V	DIR	Audio signal from DIR
60	BCK6	IN	5V	DIR	Audio signal from DIR
61					
62	KDTSEL	IN	5V		Karaoke/main data switching
63	XRST	IN	5V		Reset
64					

4-7. Small Gate Array CXD8747 (MB-78 Board IC807)

4-7-1. Block Diagram

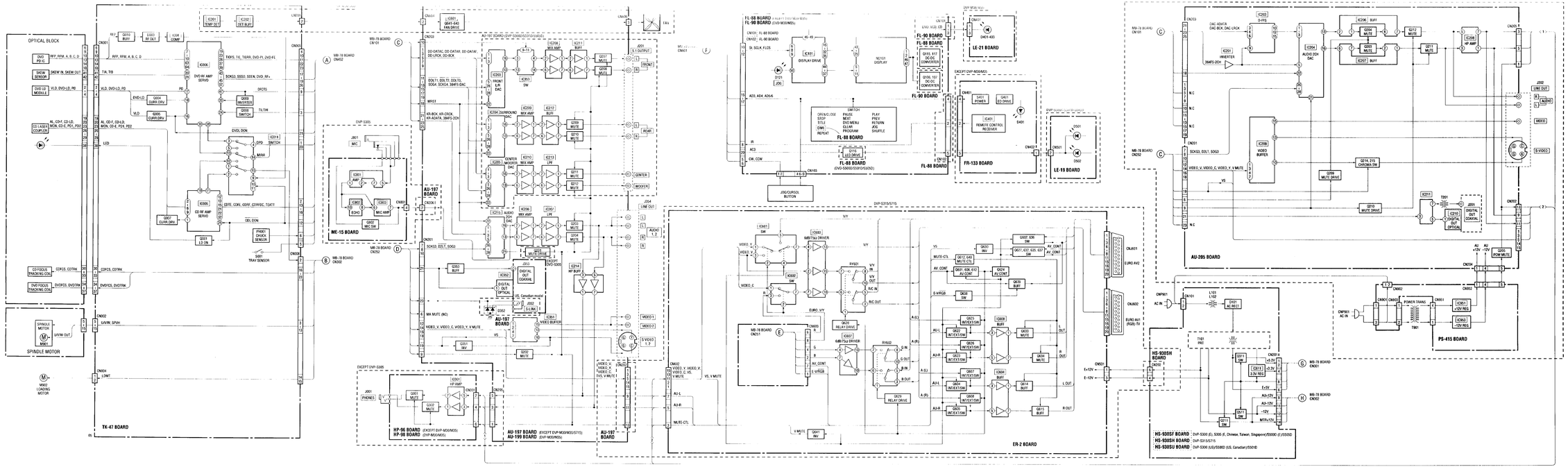


4-7-2. Pin Assignment

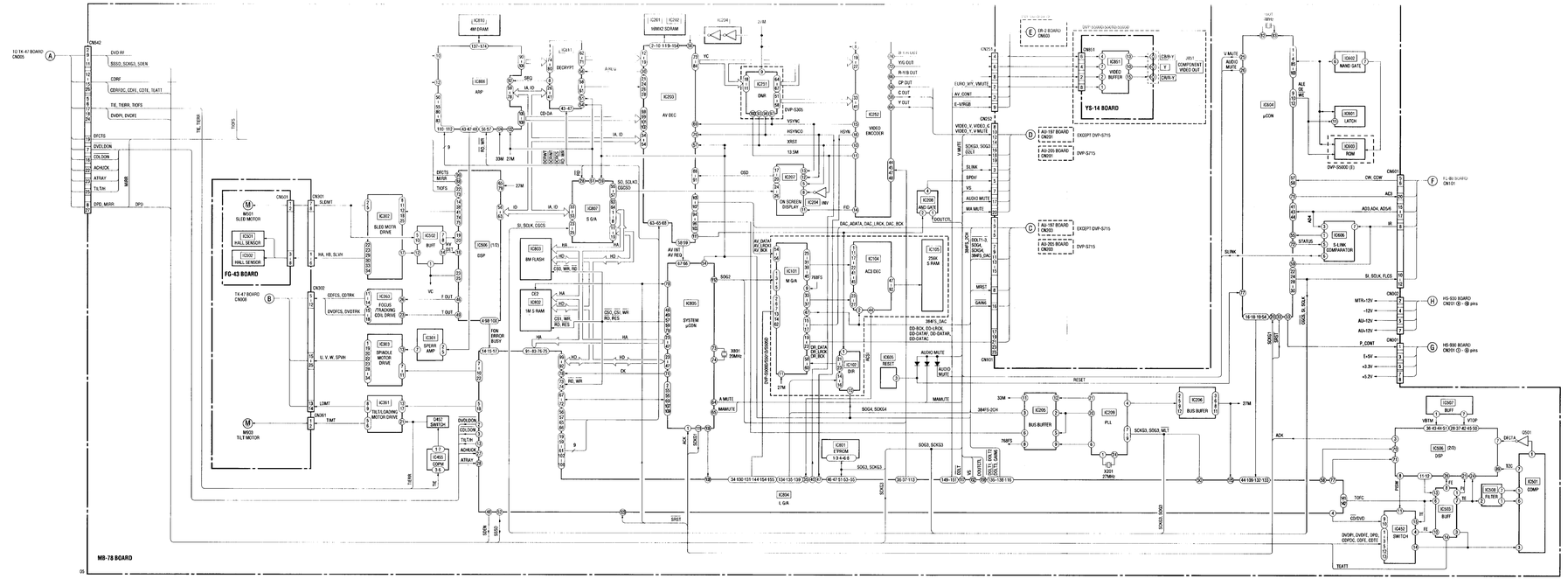
Pin No.	Signal Name	I/O	BUFF.TYPE	Pin No.	Signal Name	I/O	BUFF.TYPE
1	HA2	I	TLCHT	51	VSS		
2	HA3	I	TLCHT	52	IA1	O	B8
3	HA4	I	TLCHT	53	IA0	O	B8
4	VSS	–		54	VSS		
5	HA5	I	TLCHT	55	DO	O	B2
6	HA6	I	TLCHT	56	SCKO	O	B2
7	HA7	I	TLCHT	57	CSO	O	B2
8	HA8	I	TLCHT	58	VDD		
9	VDD	–		59	XRST	O	SCHMITT
10	VSS	–		60	VSS		
11	HD0	I/O	BD8T	61	CK	O	SCHMITT
12	HD1	I/O	BD8T	62	VDD		
13	HD2	I/O	BD8T	63	HA0	O	TLCHT
14	HD3	I/O	BD8T	64	HA1	O	TLCHT
15	VSS	–		65			
16	HD4	I/O	BD8T	66			
17	HD5	I/O	BD8T	67			
18	HD6	I/O	BD8T	68			
19	HD7	I/O	BD8T	69			
20	VSS	–		70			
21	VDD	–		71			
22	VSS	–		72			
23	CSI	I	TLCHT	73			
24	SCKI	I	SCHMITT	74			
25	DI	I	TLCHT	75			
26	VDD	–		76			
27	VSS	–		77			
28	DIR	I	TLCHT	78			
29	OE	I	TLCHT	79			
30	NC	–		80			
31	VDD	–		81			
32	VSS	–		82			
33	ID7	I/O	BD8T	83			
34	ID6	I/O	BD8T	84			
35	ID5	I/O	BD8T	85			
36	ID4	I/O	BD8T	86			
37	VSS			87			
38	ID3	I/O	BD8T	88			
39	ID2	I/O	BD8T	89			
40	ID1	I/O	BD8T	90			
41	ID0	I/O	BD8T	91			
42	VSS			92			
43	VDD			93			
44	IA8	I	B8	94			
45	IA7	I	B8	95			
46	IA6	I	B8	96			
47	IA5	I	B8	97			
48	IA4	I	B8	98			
49	IA3	I	B8	99			
50	IA2	I	B8	100			

5. OVERALL BLOCK DIAGRAM

5-1. RF, Servo, Audio, Power Block Diagram



5-2. Signal Processing Block Diagram



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